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Electrical and Electronics Systems Research Division

Oak Ridge National Laboratory Annual Progress Report for the Electric Drive Technologies Program

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October 2016

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Oak Ridge National Laboratory
Annual Progress Report
for the Electric Drive Technologies Program

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Energy Efficiency and Renewable Energy
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ACRONYMS AND ABBREVIATIONS

3-D	three-dimensional
Ag	silver
AGD	active gate drive
AM	additive manufacturing
Au	gold
AWG	American Wire Gauge
BCC	body-centered cubic
BEV	battery electric vehicle
COTS	commercial off-the-shelf
CPLD	complex programmable logic device
CPSR	constant power speed range
CTE	coefficient of thermal expansion
DBC	direct bond copper
DMOSFET	double-implanted MOSFET
DOE	US Department of Energy
DSP	digital signal processor
EDT	Electric Drive Technologies (VTO program)
emf	electromotive force
ETDS	electric traction drive system
EV	electric vehicle
Fe	iron
FEA	finite element analysis
FFT	fast Fourier transform
FWD	freewheeling diode
FY	fiscal year
GA	genetic algorithm
GaN	gallium nitride
HEV	hybrid electric vehicle
HV	high voltage

ID	inner diameter
IGBT	insulated gate bipolar transistor
IPM	interior permanent magnet
IPMSM	interior permanent magnet synchronous motor
LLG	Landau, Lifshitz, and Gilbert (in relation to micromagnetics equations)
MD	molecular dynamics
MOSFET	metal oxide semiconductor field-effect transistor
NREL	National Renewable Energy Laboratory
OBC	onboard charger
OD	outer diameter
opamp	operational amplifier
ORNL	Oak Ridge National Laboratory
PCB	printed circuit board
PE	power electronics
PM	permanent magnet
PWM	pulse width modulation
R&D	research and development
RE	rare earth
SiC	silicon carbide
SMPM	surface-mounted permanent magnet
SOI	silicon-on-insulator
SPICE	Simulation Program with Integrated Circuit Emphasis
U.S. DRIVE	United States Driving Research and Innovation for Vehicle efficiency and Energy sustainability
VTO	Vehicle Technologies Office (DOE)
WBG	wide bandgap

I. INTRODUCTION

The US Department of Energy (DOE) announced in May 2011 a new cooperative research effort comprising DOE, the US Council for Automotive Research LLC (composed of automakers Ford Motor Company, General Motors Company, and Fiat Chrysler Automotive Group), Tesla Motors, and representatives of the electric utility and petroleum industries. Known as U.S. DRIVE (Driving Research and Innovation for Vehicle efficiency and Energy sustainability), it represents DOE's commitment to developing public-private partnerships to fund high-risk–high-reward research into advanced automotive technologies. The new partnership replaces and builds upon the partnership known as FreedomCAR (derived from "Freedom" and "Cooperative Automotive Research") that ran from 2002 through 2010 and the Partnership for a New Generation of Vehicles initiative that ran from 1993 through 2001.

The Electric Drive Technologies (EDT) subprogram within the DOE Vehicle Technologies Office (VTO) provides support and guidance for many cutting-edge automotive technologies now under development. Research is focused on developing revolutionary new power electronics (PE), electric motor (EM), and electric traction drive system (ETDS) technologies that will leapfrog current on-the-road technologies, leading to lower cost and better efficiency in transforming battery energy to useful work. Research into more efficient ETDSs is also aimed at achieving a greater understanding of and improvements in the way the various new components of tomorrow's automobiles will function as a unified system to improve fuel efficiency.

In supporting the development of advanced vehicle propulsion systems, the EDT subprogram performs research and develops technologies that will significantly improve efficiency, costs, and fuel economy.

The EDT subprogram supports the efforts of the U.S. DRIVE partnership through a three-phase approach intended to

- identify overall propulsion- and vehicle-related needs by analyzing programmatic goals and reviewing industry recommendations and requirements and then developing and delivering the appropriate technical targets for systems, subsystems, and component R&D activities;
- develop, test, and validate individual subsystems and components, including EMs and PE; and
- estimate how well the components and subsystems work together in a vehicle environment or as a complete propulsion system and whether the efficiency and performance targets at the vehicle level have been achieved.

The research performed under this subprogram addresses the technical and cost barriers that currently inhibit the introduction of advanced propulsion technologies into hybrid electric vehicles (HEVs), plug-in HEVs, battery electric vehicles (BEVs), and fuel-cell-powered automobiles that meet the goals set by U.S. DRIVE.

A key element in making these advanced vehicles practical is providing an affordable ETDS. This will require attaining weight, volume, efficiency, and cost targets for the PE and EM subsystems of the ETDS. Areas of research include

- novel traction motor designs that result in increased power density and lower cost;
- inverter technologies that incorporate advanced wide bandgap (WBG) semiconductor devices to achieve higher efficiency and switching frequency while accommodating higher temperature environments and delivering higher reliability;
- converter concepts that leverage higher switching frequency semiconductors, nanocomposite magnetics, higher temperature capacitors, and novel packaging techniques that integrate more functionality into applications offering reduced size, weight, and cost;
- new onboard battery charging electronics that build from advances in converter architectures for decreased cost and size;

- more compact and higher performing thermal controls achieved through novel thermal materials and innovative packaging technologies; and
- integrated motor-inverter ETDS architectures that optimize the technical strengths of the underlying PE and electric machine subsystems.

Oak Ridge National Laboratory's (ORNL's) EDT research program conducts fundamental research; designs, builds, and evaluates hardware; and assists in the technical direction of the VTO EDT program and in setting national policy for future BEVs that addresses the overarching goal of petroleum and greenhouse gas reduction. In this role, ORNL serves on the U.S. DRIVE Electrical and Electronics Technical Team, evaluates proposals for DOE, and lends its technological expertise to the direction of projects and evaluation of developing technologies. ORNL also executes specific projects for DOE.

DOE's continuing research into advanced vehicle technologies supports the administration's goal to produce a five-passenger affordable BEV with a payback of less than 5 years and sufficient range and fast charging capability to enable average Americans everywhere to meet their daily transportation needs more conveniently and at lower cost by the year 2022.

Research Highlights

Task 2: Electric Motor Research

Task 2.1 Advanced Electric Motor Research

- Machine design and development
  - Fully optimized several non-RE motor designs including the use of ferrite magnets. Simulations indicate that DOE 2020 targets for efficiency, power density, specific power, and cost are achievable with several ORNL motor designs.
- Soft magnetic materials research and development (R&D)
  - Continued research on electrical sheet steel with high silicon (Si) content (>6%).
  - Confirmed capability for ingot-based processing vs. expensive chemical vapor deposition.
  - Developed and confirmed a novel processing technique to reduce brittleness; otherwise, the workability of high-Si steel is not suitable for mass production of motor laminations.
  - Performed extensive warm-rolling experimental trials and obtained extensive information indicating some approaches may only hold a very narrow processing window that is not robust enough for industrial exploitation.
- Advanced modeling
  - Incorporated findings from research on soft magnetic materials properties, using the newly developed characterization system, into electromagnetics modeling.
  - Developed detailed micromagnetics code and a corresponding simulation environment to study the fundamental behavior and impact of various conditions upon the magnetization and loss characteristics of electrical steel.
  - Developed a new scaling approach and implemented on the ORNL Titan supercomputer.
    - Using the scaling approach, demonstrated the transition from a monodomain to a multidomain structure as the length scale of the system is increased.
- Prototype fabrication and testing
  - Fabricated and tested a prototype ferrite PM motor.
    - Confirmed it meets DOE 2022 targets. Targets for power density, specific power, and cost were met with a peak power of 103 kW.
  - Identified key issues with magnet properties. Future studies need to be carried out to determine the availability and quality control for mass scale production.

Task 2.2 Electric Motor Performance Improvement Techniques

- Developed several reconfigurable winding approaches and demonstrated in simulations that due to the unique configurations, the switching components have lower cost and higher efficiency when compared with existing approaches.
- Designed, built, and performed benchtop testing with switching circuitry to confirm switching speed, efficiency, and effectiveness.
- Identified motor design strategies for reconfigurable windings.
- Designed a motor and demonstrated that considerable drive cycle efficiency and nearly double the power capability can be achieved with a reconfigurable winding approach.

Task 3: Power Electronics Research

Task 3.1 Electric Drive Wide Bandgap Power Electronics

- Completed static and dynamic evaluation of a 600 V trench-type silicon carbide (SiC) metal oxide semiconductor field-effect transistor (MOSFET) and a 900 V SiC double-implanted MOSFET (DMOSFET).
- Completed short circuit capability evaluation and post-failure analysis of 600 V trench-type SiC MOSFET.
- Completed module and heat sink design of a 30 kW WBG-based boost converter prototype using ORNL's WBG modules.
- Completed design, build, and test of a gate driver with improved short circuit protection function.
- Completed system level layout design of a 30 kW WBG-based liquid-cooled inverter.

Task 3.2 Wide Bandgap Converters and Chargers

- Completed design for a 6.6 kW charger converter using the latest GaN transistors manufactured by GaN Systems Inc.; a 3-D-printed cold plate; HV heavy copper PCB power planes; low-voltage (14 V), high-current PCB power planes; and a planar transformer. Completed building and testing a prototype with a power density of 10.5 kW/L and specific power of 9.6 kW/kg. Comparing the prototype to a Si-based counterpart, the GaN-based converter achieved the following:
    - 50% reduction in volume,
    - 75% reduction in weight, and
    - peak efficiency of 99% (dc/dc converter) vs. 98.4 % for the Si-based counterpart (even at a 2.5 times higher switching frequency).
- Successfully tested an integrated OBC using the 6.6 kW GaN charger converter and a 100 kW segmented traction drive system that was built using SiC MOSFETs. An improvement of 2.2 percentage points in charger system efficiency over a Si-based counterpart was observed.
- Completed testing and evaluation of magnetic cores that were 3-D printed at ORNL's additive manufacturing facility using nanocomposite magnetic powders produced by Aegis Technology Inc. Test results indicated very low core losses but a small relative permeability of 2. Future work needs to focus on increasing the relative permeability by reducing the air gaps in the cores.

Task 3.3 Gate Driver Optimization for WBG Applications

- Board Level Gate Driver Prototyping using COTS Components
    - A board level gate driver design was completed based on commercially available integrated circuits and components. SPICE (Simulation Program with Integrated Circuit Emphasis) simulations of the primary building blocks were performed using models provided by commercial suppliers.

- The design was broken into two primary building blocks: the waveform generator and the feedback circuits. Two separate designs were completed for the waveform generator. The initial design was based on steering current sources to generate the complex multistep gate drive waveform and relied on emitter-coupled logic (ECL) circuits for the fast timing requirements of this architecture. A second design allowed significantly reduced timing requirements and used a complex programmable logic device (CPLD) for timing generation coupled with four commercial gate driver integrated circuits, diode summing circuits, and a high-performance signal buffer for the gate drive. The second, less timing intensive method was selected for use in the prototype system, and each of the associated PCBs was tested and functioned as expected.

- Bench Test COTS Gate Driver with WBG Devices
  - The two circuit PCBs of the previous task were combined to drive a SiC power MOSFET. The power device source lead inductance was used as a sensing element and the associated voltage (Ldi/dt) was input to the feedback circuits to provide the gate drive rising edge threshold value (VT1) and the gate drive falling edge threshold value (VT2).
  - The SiC power MOSFET was configured to switch a clamped inductor load, allowing observation of the associated fast switching transients: dv/dt of the device drain to source voltage (VDS) and di/dt of the device drain to source current (IDS).
  - Testing of the combined system was initiated. Initial results show that although the individual system modules function as expected, additional effort is needed to fully realize a working, closed loop, benchtop prototype system.

- Iterate and Finalize Gate Driver Design
  - The experience of building and testing a closed loop, benchtop active gate drive (AGD) prototype based on COTS components supports the assertion that a design of this level of performance (fast rise and fall times, precise timing requirements, wide gate drive voltage swings) is much better suited for custom integrated circuit implementation than for COTS implementation.

- Integrated Circuit Fabrication Process Selection
  - General specifications for the target process include the availability of a number of device types including NMOS and PMOS transistors with operating voltages ≥ ~20 V, elevated temperature operation (≥175ºC), multiple metallization layers including a "thick" metal for power routing, and available cell libraries with associated SPICE models and process design kits to minimize circuit design time. Both silicon and silicon-on-insulator (SOI) processes were considered.
  - An SOI fabrication process was selected from present commercial offerings for full integration of the AGD circuit (XT06 0.6 micron Modular Trench Isolated SOI Technology Process available through X-Fab). This process includes the basic device types needed [low-, medium-, and high-voltage NMOS and PMOS transistors; three metal layers with a thick third metal layer for power routing; and an extensive library of passive devices, digital circuits, and complex analog functions including operational amplifiers (opamps), comparators, bandgap references, and analog-to-digital and digital-to-analog converters]. In addition, the process uses trench-isolated SOI technology capable of operating at temperatures up to 225ºC, making it ideal for automotive and industrial applications.

Task 4: Benchmarking, Testing, and Analysis

Task 4.1 Benchmarking EV and HEVs

- Designed, fabricated, and assembled the hardware necessary to adapt the 2016 BMW i3 transmission to the dynamometer test cell.
- Successfully integrated ORNL controls with the 2016 BMW i3 motor inverter.
- Conducted comprehensive dynamometer testing of the 2016 BMW inverter and motor to obtain efficiency maps, peak torque, peak power, and many other performance metrics.
- Confirmed published peak torque and power specifications for the 2016 BMW i3 inverter and motor.

Task 5: Advanced Packaging Technologies and Designs Research

Task 5.1 Advanced Packaging Technologies and Designs

- Developed a packaging approach of multiple chip-scale packaged gallium nitride (GaN) devices for high mechanical flatness, enabling three-dimensional (3-D) high density assembly. Fabricated and delivered GaN modules for building a 6.6 kW GaN isolation converter in project EDT 054.
- Performed electromagnetic simulation and experimental evaluation of state-of-the-art commercial power modules. Electrical performance limitations of the module packaging have been identified. Technical aspects for further improvements have been suggested.
- Designed and fabricated record-low switching ringing SiC modules. A feature inductance of 1.46 nH in a SiC power module has been realized for the first time. This will allow converter/inverter operation at higher frequencies and low electromagnetic interference (EMI) and, in turn, lower cost and high power density.
- Developed large area bonding process technologies for high reliability SiC modules. New materials and processes push SiC operating temperatures higher and increase the reliability by 3 times.
- Fabricated and delivered SiC planar-bond-all modules to the National Renewable Energy Laboratory team for thermal evaluation. The double-sided larger area bonds increase the area of the thermal path by 40%, allowing reduction of thermal resistance and reduction in cost and increase in power density.
- Established a power cycling method and test bed for power cycling tests of WBG module packaging.

Task 6: Other Support

Task 6.1 Power Electronics and Electric Motor Materials Support

- PE materials support (FY 2016 focus—sintered-silver interconnects)
  - Quantified achievable maximum strength.
  - Showed asymmetric residual stress can limit mechanical reliability.
  - Developed a proof test to identify the largest achievable interconnect size.
  - Showed shear strength was insensitive to the choice of plating, processing, and printing methods.
  - Showed sintered-Ag interconnects can be fatigue resistant.
  - Identified failure locations (weakest areas) in different sintered-Ag interconnect systems.
  - Weibull analysis and postmortem used to identify failure exclusivity and parasitics.
- EM materials support (FY 2016 focus—materials to promote thermal transfer in Cu windings)
  - Showed significant apparent thermal conductivity anisotropy of packed Cu wire.
  - Contrasted thermal conductivity test methods using Cu winding samples.
  - Used percolation theory to interpret thermal conductivity trends at higher wire-packing fractions.

II. RESEARCH AREAS

2.1 Advanced Electric Motor Research

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Abstract/Executive Summary

Almost all hybrid electric vehicle (HEV) and electric vehicle (EV) motors (machines) use permanent magnets (PMs) with rare earth (RE) materials such as neodymium and dysprosium because they facilitate the achievement of high power densities, specific powers, and efficiencies. However, there has been significant market volatility associated with RE materials in recent years, including a price increase in dysprosium by a factor of 40 within 1 year. Therefore, alternatives to RE PM motors are of very high interest to original equipment manufacturers and suppliers and will continue to be, particularly as vehicles become more electrified and uses for RE materials in other applications expand in the future. Achieving competitive performance and efficiency with alternative motor technologies having comparable mass, volume, voltage, and other key metrics requires a highly advanced multidiscipline research approach including high accuracy modeling; the research, use, and development of soft and hard magnetic materials; and comprehensive nonlinear computational optimization of geometric features and winding parameters.

Accomplishments

- Machine design and development
  - Fully optimized several non-RE motor designs including the use of ferrite magnets. Simulations indicate that DOE 2020 targets for efficiency, power density, specific power, and cost are achievable with several ORNL motor designs.
- Soft magnetic materials research and development (R&D)
  - Continued research on electrical sheet steel with high silicon (Si) content (>6%).
  - Confirmed capability for ingot-based processing vs. expensive chemical vapor deposition.
  - Developed and confirmed a novel processing technique to reduce brittleness; otherwise, the workability of high-Si steel is not suitable for mass production of motor laminations.
  - Performed extensive warm-rolling experimental trials and obtained extensive information indicating some approaches may only hold a very narrow processing window that is not robust enough for industrial exploitation.

- Advanced modeling
  - Incorporated findings from research on soft magnetic materials properties using the newly developed characterization system into electromagnetics modeling.
  - Developed detailed micromagnetics code and a corresponding simulation environment to study the fundamental behavior and impact of various conditions upon the magnetization and loss characteristics of electrical steel.
  - Developed a new scaling approach and implemented on the ORNL Titan supercomputer.
    - Using the scaling approach, demonstrated the transition from a monodomain to a multidomain structure as the length scale of the system is increased.
- Prototype fabrication and testing
  - Fabricated and tested a prototype ferrite PM motor.
    - Confirmed it meets DOE 2022 targets. Targets for power density, specific power, and cost were met with a peak power of 103 kW.
  - Identified key issues with magnet properties. Future studies need to be carried out to determine the availability and quality control for mass scale production.

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Introduction

As the electric motor is one of the main components of HEV and EV drivetrains, improving efficiency, performance, and cost-effectiveness is crucial to the hybridization and electrification of vehicles. PM motors are not easily surpassed in terms of efficiency, power density, and specific power, and therefore almost all HEVs and EVs use them. However, the cost of RE PM material accounts for at least 40% of the entire motor cost, and the high and unstable costs of RE materials have caused automotive manufacturers and suppliers around the world to seek alternative non-RE motor technologies that facilitate cost-effectiveness as HEV and EV markets continue to expand. Therefore, the development of alternative non-RE motor technologies plays an important role in future economic stability and achieving clean energy goals and energy independence.

Approach

The primary objective of this project is to develop low-cost non–RE motor solutions with high power density, specific power, and efficiency. Figure 1 illustrates the overall structure of the efforts in the project. Key efforts of the project include conventional motor design techniques, advanced motor modeling, motor materials research, and empirical verification.

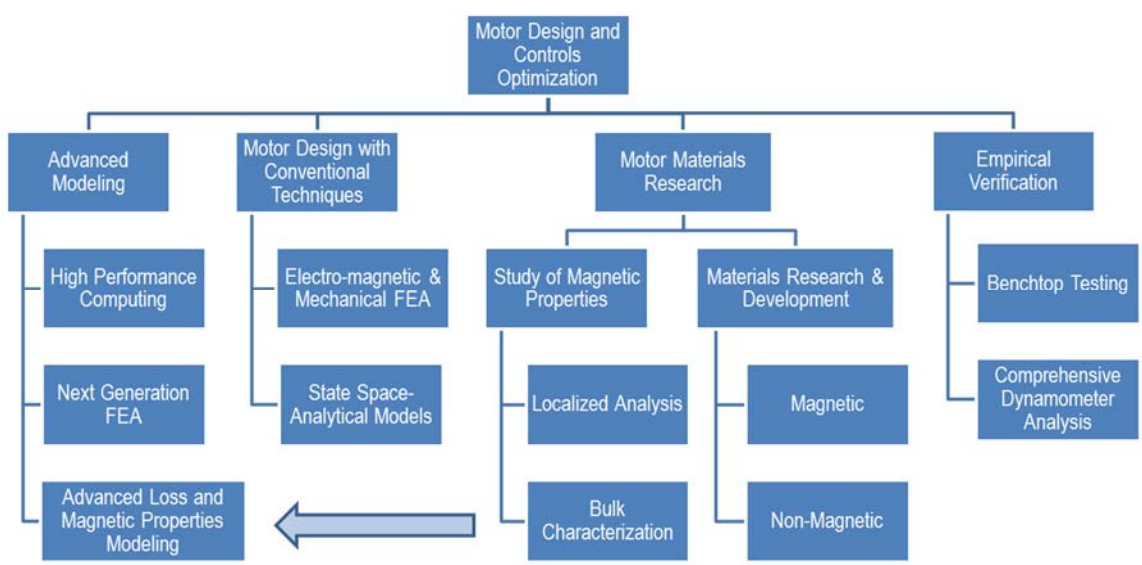


Figure 1: Motor research thrust areas and project structure.

In the initial stages of this project, many types of novel electric motor designs were developed and considered in coarse simulations to identify the most feasible designs with high potential for commercialization. The wide range of motor types studied includes field excitation, synchronous reluctance, non-RE PM motors, and combinations of these machine types. Proof-of-principle components were built and tested to serve as a feedback mechanism for novel motor development and fundamental soft magnetic materials research. Novel motor designs were developed and optimized using high performance computing techniques, beginning with implementation and modeling on parallelized workstations, and preparations are under way for the use of computational clusters and ultimately the supercomputer at the computational facility at ORNL. Findings from fundamental magnetic materials research are being incorporated into new modeling tools to improve accuracy, and this has been greatly facilitated with parallelized computing.

In addition to novel motor and controls development, the development and use of new materials and materials processing techniques was carried out to improve magnetization and/or efficiency characteristics of soft magnetic materials (e.g., electrical steel). This effort is being conducted in coordination with the propulsion materials program. Additionally, new materials or manufacturing techniques were studied and used to obtain improvements in manufacturability (cost reduction), cooling (collaborating with the National Renewable Energy Laboratory), and improved mechanical integrity.

To improve motor modeling accuracy and complement new materials and processing developments, fundamental research was conducted to study the phenomena behind magnetization and loss characteristics of soft magnetic materials in electric motors, details that are still not fully quantified or understood in the scientific community. For example, residual stresses or induced stresses incurred during manufacturing or motor operation have a considerable impact upon losses and permeability. Additionally, temperature, pulse width modulation excitation, and other factors impact the magnetic properties in a way that is not considered or modeled with conventional finite element analysis (FEA) tools. These studies supported the development of high fidelity models and modeling tools, which are particularly important as high performance computing is used in the optimization of detailed geometric features to achieve high power density, specific power, efficiency, and cost-effectiveness. After comprehensive optimization, a ferrite PM motor was fabricated and analyzed in an ORNL dynamometer test cell.

Results and Discussion

Motor design optimization in FY 2016 was conducted with commercial FEA packages, in-house custom design tools, and other software packages for parametric optimization algorithms and state space simulations. Progress and results in the area of motor design are discussed in the following sections, including parallel efforts in materials R&D. These parallel efforts ultimately support improving motor designs through developing or facilitating the use of more efficient materials and conducting fundamental research to improve modeling accuracy.

Modeling of Magnetic Domains

In soft magnetic materials, such as iron (Fe) and Fe-Si alloys (electrical steels) used in motor laminations, the magnetic behavior during operation is linked to the evolution of the magnetic domain structure during external magnetization and demagnetization cycles. The effect of elastic strains and pinning due to nonmagnetic defects in the steel microstructure significantly influence the temporal evolution of the domain structure and hence the magnetic response. A simulation effort at the mesoscale was undertaken to quantify the magnetic behavior under such conditions and to provide realistic magnetic constitutive behavior to continuum level simulations of motor performance. Current approaches to simulate domain structure evolution involve solution to the micro-magnetics equations proposed by Landau, Lifshitz, and Gilbert (LLG). The LLG approach is based on treating magnetism as a continuous vector field and solving the temporal evolution of the effective magnetic field to minimize total magnetic energy. Typically, solution techniques involve the use of a phase field approach with a diffuse interface between two magnetic domains where the magnetization changes continuously. However, phase field approaches require many parameters that are based on averaging atomic level quantities. In many cases such parameters are not readily available. On the other hand, simulations of nanoscale magnetic behavior have used discrete magnetic moments at the atomistic scale to predict collective evolution of magnetic domains using atomistic techniques. Such an approach has been used, for example, in simulating magnetic domain formation in nanoscale thin films and magnetic switching in nanoscale devices.

In either of the two approaches, the length scale over which the simulations can be carried out is severely limited by the ability to calculate the magnetic dipole-dipole interaction energy that involves long-range interaction terms for every volume element in the simulation domain. The general strategy has been to use simplifications based on the use of fast Fourier transforms (FFTs) that necessitate the use of periodic boundary conditions that may not be realistic in many cases. An alternative technique based on the fast multipole method has been widely used in similar problems but has not been readily adopted in micro-magnetics simulations. It is necessary to perform the simulations at length scales of several micrometers because the magnetic domains that form as a result of a competition between magnetic exchange energy and the dipole-dipole interaction energy exist only at such length scales. One approach to overcome this problem and observe domains at smaller length scales has been to scale down the exchange energy and establish a relationship between the reduced length scale and the equivalent realistic length scale. However, a universal relationship between the two has not been established.

In pursuit of the goals and objectives of this project, a new scaling approach has been successfully developed and has been shown to demonstrate the transition from a monodomain to a multidomain structure as the length scale of the system is increased. Such an approach has been made possible by the use of high performance computing in the calculation of the dipole-dipole interaction energy and exchange energy in a series of domain sizes. The scaling of the exchange energy and the dipole energy as a function of the system size is shown in Figure 2. The application of the scaling laws shows the transition from a monodomain structure at small simulation volumes, shown in Figure 3(a), to the formation of vortex type structures in larger volumes, shown in Figure 3(b). The simulations are also able to capture the experimentally measured domain wall thicknesses in Fe-3%Si steel. The simulations are being extended to polycrystalline grain structures to capture magnetization and demagnetization curves as a function of grain orientations.

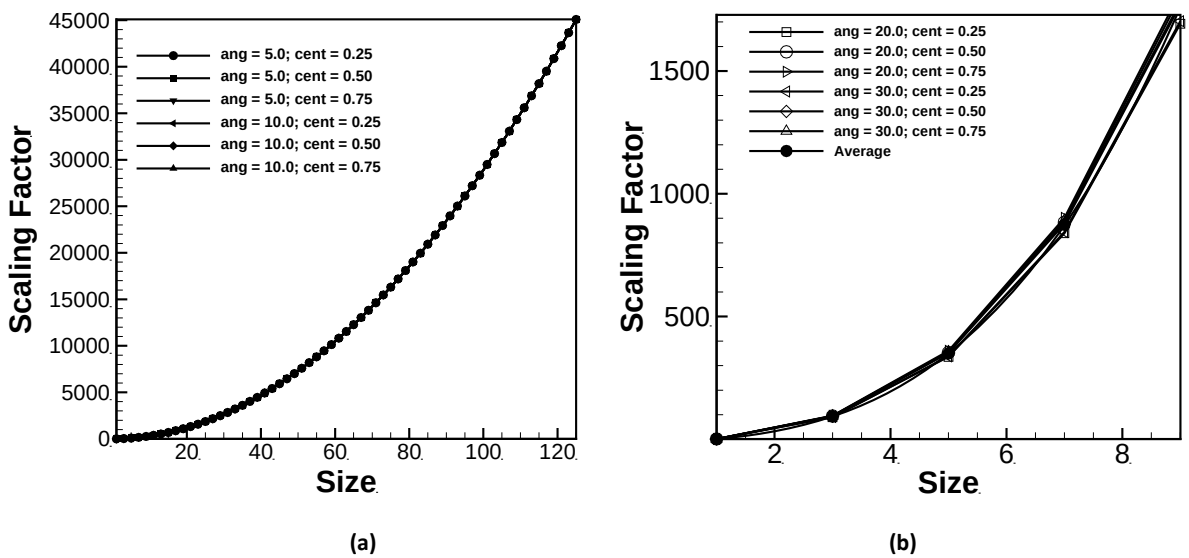
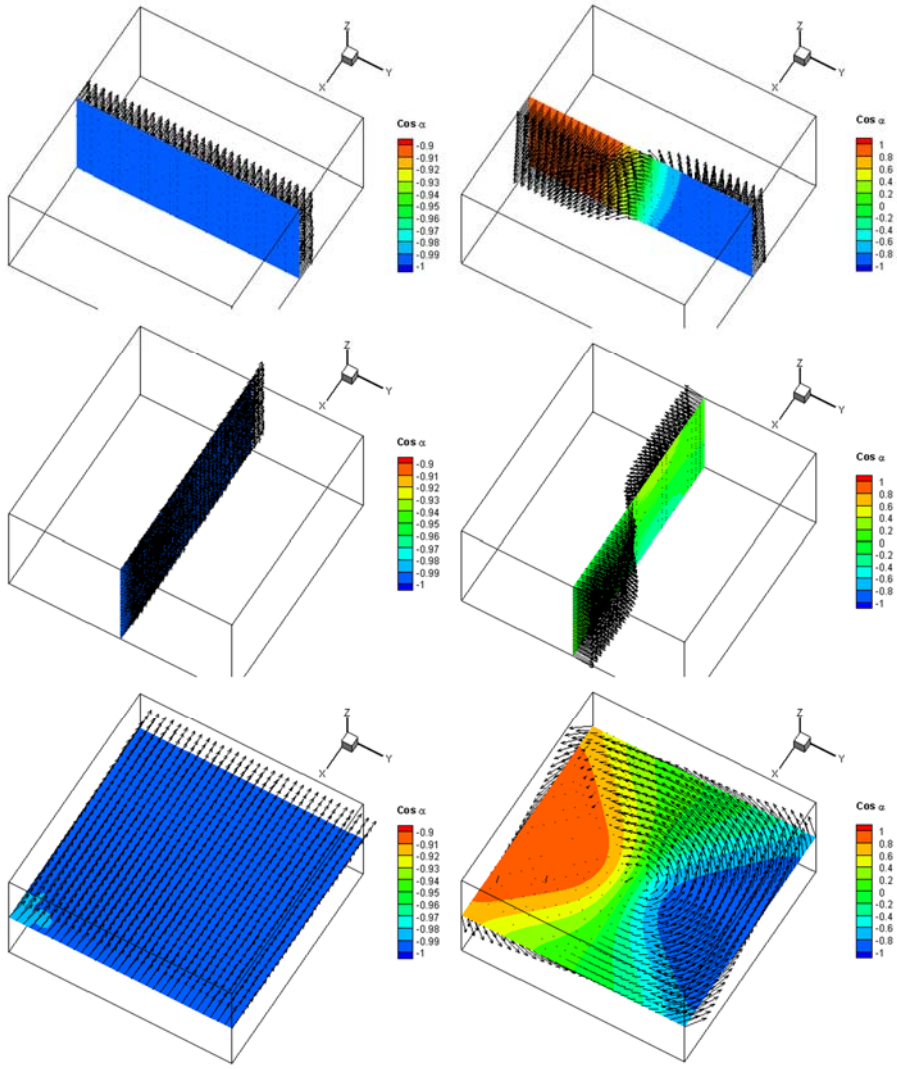


Figure 2: Scaling of the exchange energy (a) and dipole-dipole interaction energy (b) as a function of the system size for body-centered cubic iron.



(a) (b)

Figure 3: Evolution of the magnetic moment distribution as a function of system size showing the transition from monodomain (a) to vortex structure (b). [Note: Size in (a) = 1 (9.152 × 9.152 × 4.576 nm3) and in (b) = 51 (467 × 467 × 236.5 nm^3).]

High Efficiency Steel Research: Thermomechanical Processing of Fe–6% Si alloys

Increasing the Si content in soft magnetic steel (e.g., Fe-Si) to 6% can increase resistivity and reduce losses by about 35%. However, with high Si content, conventional stamping of laminations is no longer possible because the material becomes too brittle. Efforts were made on this project to develop a deeper understanding of the driving mechanisms, explore additives to improve ductility from ingot form, and develop modifications to conventional thermomechanical processes. Iron-silicon alloys containing greater than 3 wt % Si undergo congruent ordering on cooling from the processing temperature. This is a second order transformation that involves local hopping of the Si atoms to the body center of the body-centered cubic (BCC) unit cells of iron and, therefore, a statistically higher occupancy of the body center compared to the corners of the BCC unit cell. However, molecular dynamics (MD) simulations using a recently formulated modified embedded atom potential for the Fe-Si system have shown the significantly higher yield strength of Fe-Si alloys in the congruently ordered condition compared to a disordered state. The summary of MD simulations is shown in Figure 4.

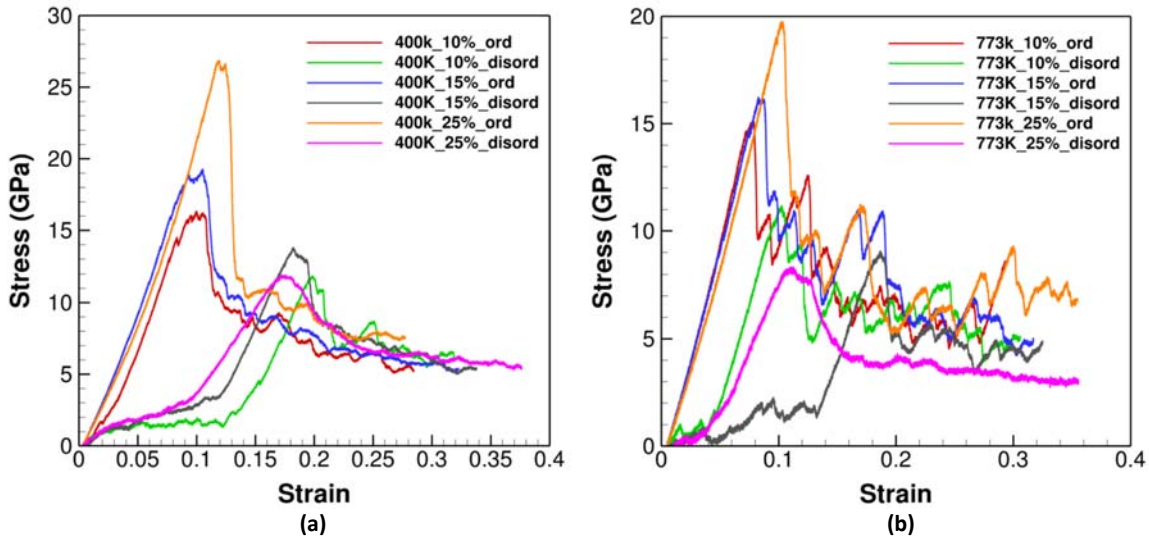


Figure 4: MD simulations of the deformation of Fe-Si single crystals containing 10 to 25 at. % (5 to 12 wt %) Si at (a) 400 K and (b) 773 K.

The ordering of Si atoms cannot be suppressed at the cooling rates encountered in conventional thermomechanical processing. However, it has been well documented in the literature that warm working the alloy in the temperature range from 400°C to 550°C followed by normal process cooling can recover the ductility of the alloy at room temperature and promote subsequent cold rolling. There is also sufficient evidence in the literature that large deformation around 900°C, which is higher than the ordering temperature of the alloy, followed by forced cooling allows cold rolling if it is performed without long holding periods at room temperature (less than 4 h). In FY 2016, a number of laboratory trials and rolling experiments were performed using Fe-6Si and Fe-6.5S alloys, with or without parts-per-million levels of boron, to test the above, suggested routes. The hot-working temperature, the extent of deformation, and the hold time and temperature were systematically varied. So far these efforts have had limited success whereas warm rolling at 300°C–350°C followed by cold rolling resulted in 0.8 mm thick sheet with significant extent of edge cracking. All of the other parametric studies failed, with the material exhibiting significant cracking during cold rolling. Therefore, it has been concluded that the above approaches may only hold a very narrow processing window that is not robust enough for industrial exploitation. Alloying strategies are being considered to either suppress the kinetics of ordering or completely eliminate ordering in Fe-Si-X alloys while simultaneously maintaining the magnetic properties and the required resistivity levels for high-frequency motor applications.

Motor Design and Power Density Optimization of a Ferrite Interior Permanent Magnet

The development of unconventional motor technologies was accomplished by improvising upon promising technologies from previous work and initiating work on novel motor concepts. Previous research includes the design of various motor types, including induction motors, switched reluctance motors, hybrid excitation motors, and flux coupling/field coil machines. Novel motor designs were generated and simulated, with consideration of various machine types such as switched reluctance, hybrid PM excitation, synchronous reluctance, and field coil excitation. Recent designs include the use of ferrite magnets for improved power density. ORNL used advanced optimization algorithms to optimize motor design and controls. Electromagnetic FEA tools were used to implement basic models to determine performance and operational characteristics of new motor designs. Analytical models were used to determine additional performance metrics and associated control methods.

Spoke-type ferrite interior permanent magnets (IPMs) have received attention in recent years due to the push for reduced RE content in PMs. The spoke topology refers to a method of arranging the magnets on the rotor so the flux is produced and concentrated in the tangential direction before crossing the air gap to the stator. This topology allows a great increase in the magnet mass on the rotor and, because of this, is promising for ferrite-based machines intended to replace those using NdFeB magnets. However, most ferrite-based spoke IPMs explored in the literature use expensive techniques to reduce leakage flux (e.g., keyed beryllium hubs), result in limited speed ratings (less than 8,000 rpm, free rotor pole pieces with axial support posts), use more

expensive high strength steel, or have not been optimized over a wide variety of parameters. This project has focused on optimizing a spoke-type machine to achieve an understanding of the achievable power density of ferrite-based IPMs. We consider a model with 13 parameters, 7 of which are free, 4 of which are fixed, and 2 of which are implicitly constrained. The main materials selected, namely the PMs and steel material, are also fixed in advance.

Free Parameters

The seven free dimensional parameters allowed to vary in the optimization routine are shown in Figure 5(a) and the overall base motor design is shown in Figure 5(b). Six of the seven parameters in the models are dimensionless, allowed to vary from 0 to 1, and normalized to the rotor outer diameter. The scale-dependent parameters are the stator back iron thickness, stator tooth length, stator tooth width, magnet thickness, rotor q-axis tooth width, and rotor d-axis depth. This is done so that models with the same unitless parameters are roughly comparable on a per-unit basis (with the unit being the rotor outer diameter).

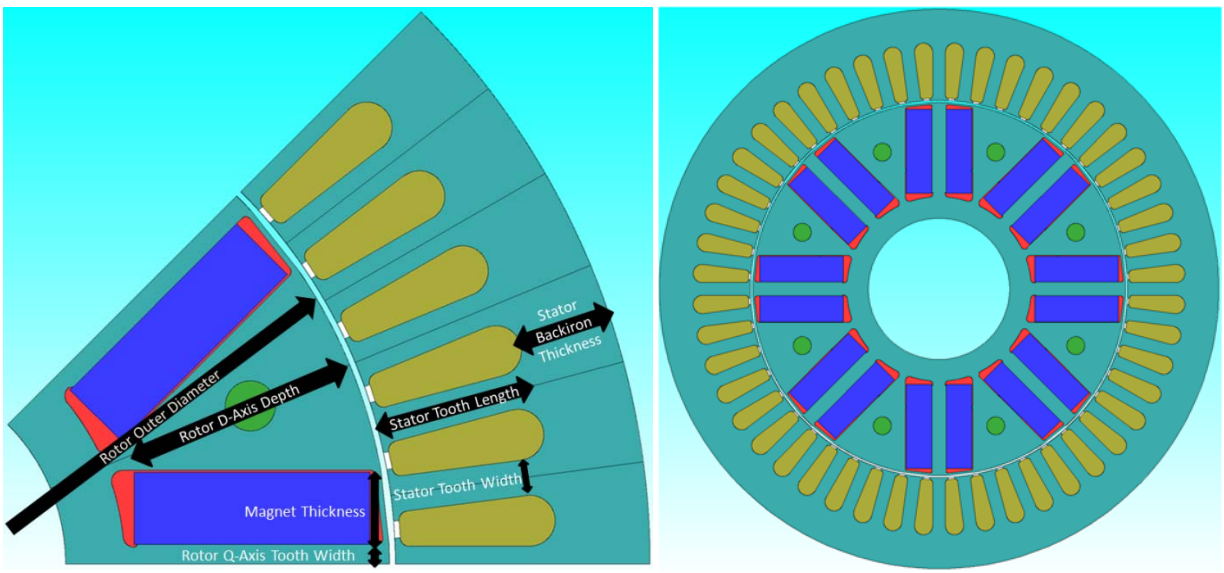


Figure 5: Free optimization parameters of a ferrite IPM (a) and full basic design (b).

Fixed Parameters

In addition to the free parameters, two parameters are fixed. First, the maximum speed of the machine is fixed at 14,000 rpm, but as part of our initial investigations, the maximum speed was allowed to vary from 7,000 rpm to 14,000 rpm. However, it was quickly apparent that the maximum power density designs converged on high speed operation, even when mechanical constraints were considered. Second, the maximum current density was limited to 13 Arms/mm^2 averaged over the slot area, or about 29 Arms/mm^2 in the conductors themselves. This is about the same as the 2010 Prius motor, and a relatively large value that has been observed to limit the peak torque of the delivery time in practice. Nevertheless, this is necessary for achieving high power densities in RE-free machines. Because of this, cooling must be designed carefully in production vehicles. The final two fixed parameters are the inverter voltage and current rating. These were set at 650 Vdc and 200 Arms, respectively. The models are evaluated by applying a fixed current density to the slot. A posteriori determination of the number of turns is made using the slot geometry, maximum current density, and an assumed slot fill factor of 45% (similar to the 2010 Toyota Prius).

Implicitly Constrained Parameters

Torque-Constrained Stack Length

The optimization procedure used two-dimensional FEA to determine design performance. Ignoring end effects, this gives an effective torque per unit length for a given design. This allows for all candidate designs to be sized to address the low speed torque requirements. In the initial design, a power level of 60 kW from

2,800 rpm to 14,000 rpm was targeted. A low speed torque of 225 Nm was chosen to give a 10% margin of error. Later, magnet material selection was changed (discussed later) and 55 kW/206 Nm was targeted.

Mechanically Constrained D-Axis Bridge Width

The thickness of the bridge on the d-axis of the rotor connecting the d-axis pole piece to the rotor hub and supporting the magnets is constrained by the yield strength of the lamination material. In particular, the bridge thickness was constrained to keep the Von Mises stress at 14,000 rpm to below half of the material yield stress. A thinner bridge reduces the leakage flux, so it is more advantageous magnetically. On the other hand, repeatedly cycling loads between low and high stress levels can induce fatigue-related failures, so it is desirable to keep the stress levels as low as possible. A rough rule of thumb is to keep the peak stress below half of the yield strength of the material. This is equivalent to having a safety margin of 2. A novel method for sizing the bridge was developed to avoid performing mechanical finite element simulations for every design.

Material Selection

The two main materials that must be selected for this design are the steel laminations and ferrite PM material. For the laminations, JFE Steel grade 35JN210 was selected. This is the lowest loss variety lamination of JFE's standard grade nonoriented steel. Most importantly, however, it has the highest rated yield strength out of all the grades at 450 MPa. This allows for the minimization of the rotor d-axis support bridge width, thus minimizing the main leakage flux path.

During initial optimization runs, Hitachi NMF-12J ferrites were used as the PM material. These magnets substitute lanthanum and cobalt for strontium/barium to improve the temperature stability of the demagnetization characteristics. This has the additional effect of greatly improving the magnet coercivity. The drawback is the relatively high cost of lanthanum and cobalt compared to strontium and barium. Unfortunately, after contacting suppliers for several months, we were unable to find a source for prototype magnet material. After additional investigations, a substitute material from two separate suppliers was found. The ferrite grade is called Y40 and is part of a standard that is emerging in popularity in Europe and China, and to a lesser extent the United States. The so-called Y-standard specifies magnets of much higher energy product than can be found using the C-standard typically used in the United States. Typical properties of both magnet types are given in Table 1. At 20°C, the properties are quite similar.

Table 1: Typical ferrite magnet properties at 20°C

Material	Br (T)	Hci (kA/m)	Hcj (kA/m)	BHmax (kJ/m3)
NMF-12J	0.44	430	340	37.4
Y40	0.44	340	330	37.5

Design for Manufacturability

The magnets are designed to slip into their rotor slots with a small clearance and are potted in place with a strong epoxy. In the prototype rotor, the magnets slipped in and out of the slot relatively easily while magnetized. In the final assembly step, the bottom of the rotor was taped and sealed. A small amount of epoxy-based material was placed in the bottom of the slot and the magnet was pressed into place. The excess material was cleaned off the surface before curing. Careful metering of the amount of epoxy would allow either manual or automated rotor assembly with ease. It should be noted that, although the epoxy is expected to improve the mechanical strength of the rotor, it has not been relied upon when calculating the mechanical safety margin of the rotor. That is to say, the epoxy may de-bond from the laminations or magnets without causing the rotor to fail. The rotor q-axis bridge is designed to support the full load of the rotor pole face and magnets with an adequate safety margin.

Optimization

Model Evaluation

Two key performance criteria must be evaluated for each model: maximum torque and peak power at maximum speed. Theoretically, the maximum torque capability at 2,800 rpm must be evaluated. In practice,

however, designs around the optimum were able to deliver peak torque well above this speed. A truly accurate evaluation of the peak torque would also require determination of the current angle that produces this value. It can be shown using simply D-Q torque models, however, that for machines with significant reluctance torque, the maximum current angle does not deviate far from 45 (or 135) degrees. The error is insignificant when it comes to differentiating between designs and is easily accounted for by small increases in the stack length. Similarly, the maximum power at peak speed would require determination of the current vector, both magnitude and direction, that produces this value. Instead of performing this expensive operation for each design, a simpler approach was implemented that gives a lower bound on the maximum power. This is done through a determination of the characteristic current by simulating a few (usually two) different current vector magnitudes aligned with the negative d-axis. Along with the inverter voltage rating, the machine characteristic current gives the asymptotic peak power of the machine as the speed becomes large. When searching for a machine with an asymptotic power of 55 kW or 60 kW, it is guaranteed that the peak power at 14,000 rpm will be larger than this value. A tighter value can be obtained by iteratively reducing the required asymptotic value until the power at maximum speed is equal to the targeted value.

Optimization Algorithm

A novel guided random search method was implemented to optimize the design. To start, population of candidate designs is drawn randomly from a joint Gaussian distribution with a given mean and standard deviation. The mean of the distribution is moved from the value to the design on the Pareto front closest to the target values. A sigmoid function is used to update the standard deviations of the individual parameters based on the distance between the previous mean and the updated mean. The sigmoid function is calibrated so that the "Gaussian search spheroid" expands when searching far away from the optimum, contracts when searching close to the optimum, and changes shape when certain parameters are more influential on the optimal design than others. The adaptability of both scale and directionality results in a quickly converging algorithm.

Results and Trends

Initial optimization runs involved the use of Hitachi NMF-12J ferrite magnets. The population size of the algorithm was set to 72. Fourteen iterations were performed for a total of 1008 model evaluations. All optimization runs were performed assuming a temperature of 100°C. A scatter plot of the active volume versus the asymptotic power for the candidate designs is shown in Figure 6. The minimum volume design meeting the 60 kW target is marked with a black "X." Interesting trends are observed in the optimization results. In Figure 7 a scatter plot of the power density versus volume is shown for a subset of the candidate designs. Around the optimal design, where the Pareto front is well resolved, a trend of increasing power density with increasing volume can be observed. This implies that a higher power density can generally be achieved as the targeted power rating increases

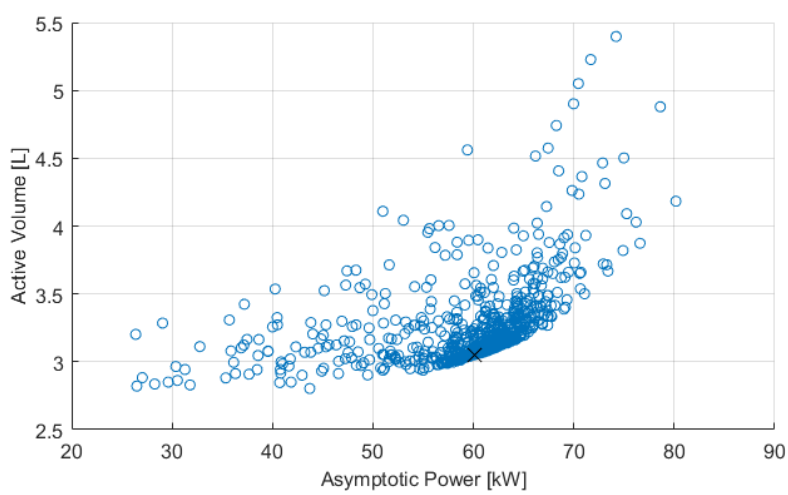


Figure 6: Optimization trend: Volume versus asymptotic power for 1008 candidate designs.

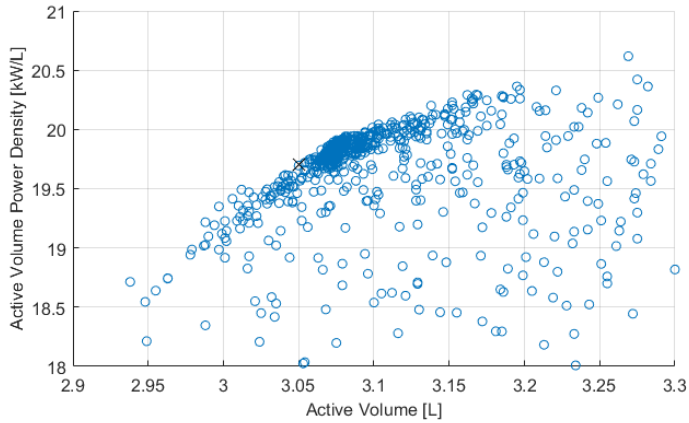


Figure 7: Optimization trend: Active volume power density versus active volume.

A scatter plot of the power density versus length to stator outer diameter (L/D) ratio of a subset of the candidate designs is shown in Figure 8. The observed trend here is increasing power density with increasing L/D ratio. This implies that, for electric machines with weaker magnets, it is much easier to achieve higher power densities in more elongated designs. For example, the 2010 Toyota Prius has an L/D ratio of about 0.19, whereas this optimal design has a ratio of nearly 0.49.

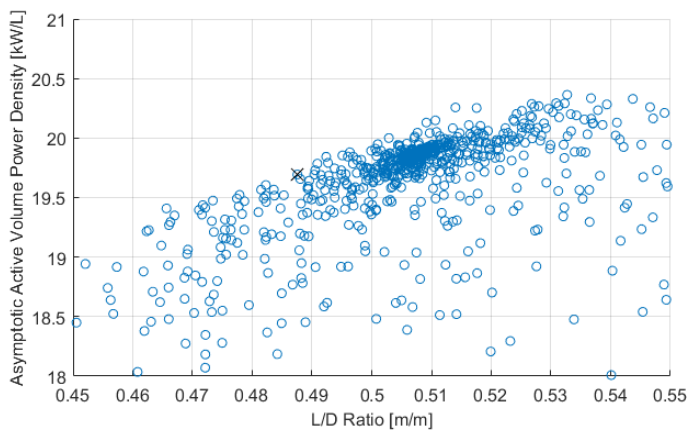


Figure 8: Optimization trend: Active volume power density versus L/D ratio.

A similar process was undertaken after the magnet material was switched from NMF-12J to Y40. The peak power/torque requirements were reduced to 55 kW/206 Nm, and the asymptotic power was modified to give a true top speed power closer to 55 kW. Even with these reductions, the machine volume ended up increasing slightly to 3.3 L (active) due to Y40's larger temperature coefficients compared to the lanthanum-cobalt-based NMF-12J. All optimizations were performed assuming a 100°C magnet temperature. A full characterization of the Y40 design was performed to verify the expected performance of the design based on the minimum number of simulations used during optimization. A motor efficiency map for an operating temperature of 100°C is provided in Figure 9. Notable in these plots are the broad regions of 96% efficiency, especially at high speed. This is a consequence of the relatively weak Y40 magnets (compared to NdFeB), which induce far less core losses at higher speeds.

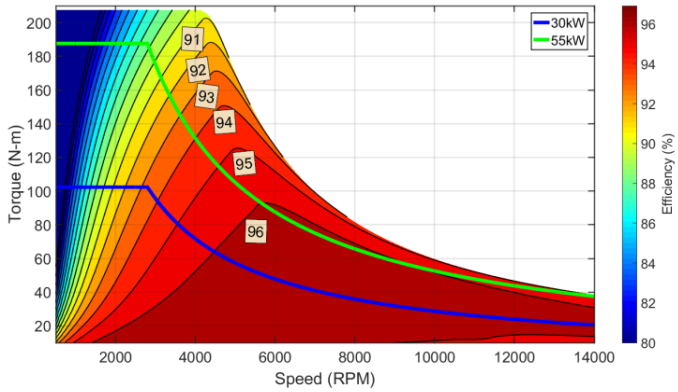
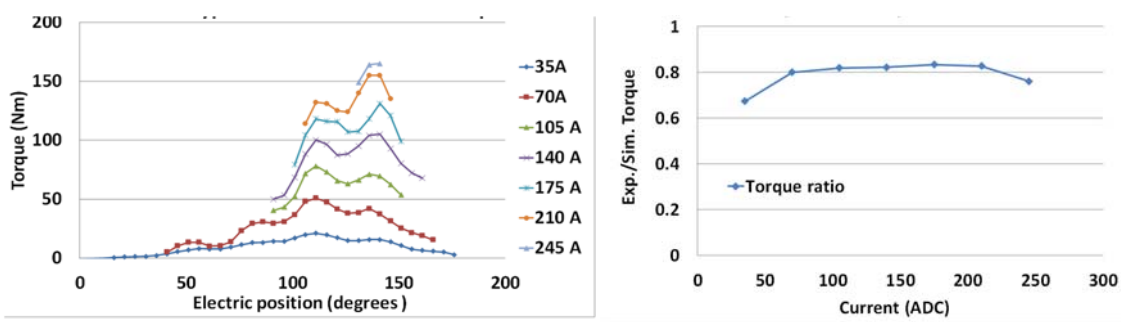


Figure 9: Simulated torque-speed efficiency map.

Prototype Fabrication and Dynamometer Testing

Magnets were ordered from two different suppliers. Before assembly of the rotor, the magnets were preliminarily tested using a Gauss probe and a crude push-force test. The actual magnet strength differed significantly between the different suppliers, with one providing consistently lower strength magnets than the other. Unfortunately, the higher strength magnets were still significantly weaker than the datasheet values. Gauss probe measurements indicated that free-air measurements were about 80% of what was expected, and later, back electromotive force (back-emf) tests resulted in similar indications of inferior properties (80%).

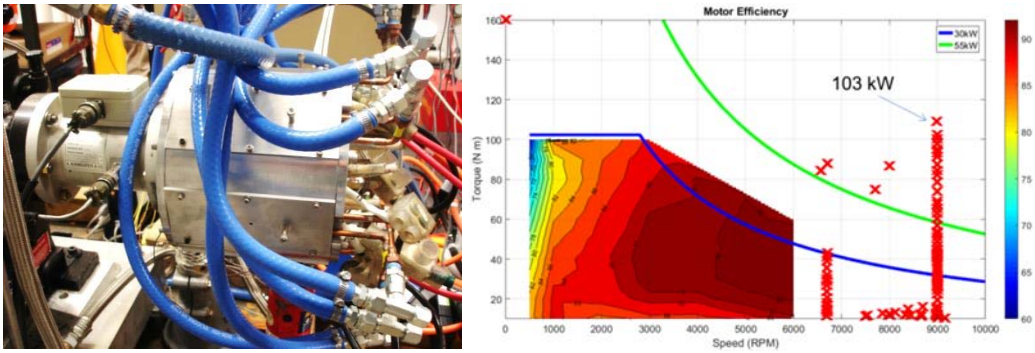
The measured locked rotor torque versus electrical position for various currents is in Figure 10(a). A torque of 165 Nm was observed with a current level of 245 Adc (~173 Arms equivalent), and the motor was designed to operate at about 200 Arms. These results also indicate degradations in magnet performance, and a slight demagnetization occurred during these tests. The ratio of experimental locked rotor torque to simulated torque is shown in Figure 10(b). It can be seen that the discrepancy is about 20%. While some relative decrease in torque/current was expected with increasing current, the highest current (245 A) resulted in demagnetization. Back-emf tests following locked rotor tests indicated significant demagnetization. With the brief application of high currents, the magnets were restored to about 80% of their original strength, which resulted in all tests being completed with magnets having residual flux density at about 65% of what was anticipated. The issue with magnet quality and availability is being investigated further, as samples are being made for four-quadrant testing with a hysteresis graph.



(a) (b)

Figure 10: Locked rotor torque versus current test results (a) and ratio of experimental and simulated results (b).

An image of the prototype ferrite PM motor on the dynamometer is shown Figure 11(a). Despite significant issues with magnet performance, encouraging test results were obtained. High torque testing was avoided until high speed and high power measurements were made. Efficiency mapping for moderate torques and speeds are indicated in the graph shown in Figure 11(b). Other high performance measurements are also indicated with an overlay of red "x" markers, including the highest measured power of 103 kW at 9,000 rpm. The efficiency is above 90% for most operation points above 2,500 rpm, and the overall efficiency is considerably lower than expected due to the magnet flux density being ~65% of what was originally anticipated.



(a) (b)

Figure 11: Ferrite PM prototype on dynamometer (a) and experimental test results (b).

Conclusions and Future Directions

The simulated peak power of the ferrite motor was 60 kW at 2,800 rpm, over 90 kW at about 4,500 rpm, and greater than 55 kW at 14,000 rpm. A summary of key simulated and measured performance metrics is given in Table 2. Detailed cost estimation efforts were conducted that include consideration of magnet grinding cost. Additionally, metrics associated with the measured power of 103 kW are also included in the table. It was estimated that the total motor material and manufacturing cost ranges from about $200 to $450. DOE 2022 targets for power density, specific power, and cost are 5.7 kW/L, 1.6 kW/kg, and $4.7/kW, respectively. It can be seen that the DOE cost and power targets are met by the ferrite motor, although the motor has limited torque production capability.

Table 2: Simulated and measured performance data

Speed (rpm)	Peak Power (kW)	Power Density (kW/L)	Specific Power (kW/kg)	$/kW (Low)	$/kW (High)
DOE 2022 Target	55	5.7	1.6	4.7	4.7
2,800 (simulated)	60.8	6.08	1.83	3.3	7.4
4,500 (simulated)	93.5	9.35	2.81	2.1	4.8
9,000 (measured)	103	10.3	3.10	1.9	4.4

This work has demonstrated that it is possible to design a ferrite-based IPM motor that achieves power density targets without using expensive rotor construction techniques or exotic lamination materials. The test results and magnet procurement have demonstrated that some difficulties still remain with magnet sourcing and quality. As the interest in ferrite-magnet-based motors continues to increase, the Y-series ferrites are likely to gain popularity. There is little public, independent information on these magnets and it will be useful to perform a more thorough investigation in the future.

FY 2016 Presentations/Publications/Patents

1. T. Burress, et al., “Advanced Electric Motor Development” presented at the DOE Vehicle Technologies Office 2016 Annual Merit Review, June 2016, Washington, DC.

2.2 Electric Motor Performance Improvements Techniques

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Contract No.: DE-AC05-00OR22725

Abstract/Executive Summary

This project focuses on the development of methods to reduce motor drive system size, mass, and cost while improving efficiency throughout the various speed, torque, and power operation regions of hybrid and electric vehicles. These methods are intended to be applicable to many types of motors, and are particularly useful for permanent magnet (PM) motor designs with reduced or no rare-earth material or even induction- or reluctance-based motors. While various methods were investigated, most research focused on reconfigurable (switched) winding approaches to achieve the targeted metrics. Various reconfigurable winding approaches were developed and comparisons are provided with those found in the literature. Additionally, design strategies for reducing magnet volume were developed and exemplary designs are provided.

Accomplishments

- Developed several reconfigurable winding approaches and demonstrated in simulations that due to the unique configurations, the switching components have lower cost and higher efficiency when compared with existing approaches.
- Designed, built, and performed benchtop testing with switching circuitry to confirm switching speed, efficiency, and effectiveness.
- Identified motor design strategies for reconfigurable windings.
- Designed a motor and demonstrated that considerable drive cycle efficiency and nearly double the power capability can be achieved with a reconfigurable winding approach.

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Introduction

Since hybrid electric vehicles (HEVs) were introduced to the market in the late 1990s, high power electric machines for automotive applications have been heavily researched. Automotive manufacturers most commonly use interior permanent magnet synchronous motors (IPMSMs) for electric vehicles (EVs) (including HEVs, battery EVs, and range-extended EVs) because of their high efficiency and high power density despite the high costs associated with rare earth (RE) PM material. Motors with low-cost magnets or no magnets (such as synchronous reluctance or induction motors) struggle to match torque and power performance when compared to an RE PM motor of similar size and mass. The first of two main efforts on this

project was the research and development of methods and switching arrangements to expand the operation range and efficiency of motors for operation throughout various drive cycles. This includes considerations of cost, complexity, and manufacturability as a part of the system optimization. The second primary effort on the project involves the development of design strategies for reducing PM volume using reconfigurable windings. While reconfigurable winding approaches with IPMSMs were researched on this project, these approaches are applicable to almost all types of electric machines for both motoring and generating applications.

Approach

The efficiency map of an IPMSM for a commercial HEV [1] and qualitative output characteristics of an IPMSM with different winding configurations are shown in Figure 1. At low speeds, the motor currents can be selected according to the maximum torque per ampere rule so that the stator current in the motor is minimal, thus keeping the switching and conduction losses of the inverter and copper loss motor low. At higher speeds, flux weakening (FW) operation is implemented to weaken the permanent flux so that restraints due to higher back electromotive force (back-emf) can be mitigated. Because total current from the inverter is limited, the torque-producing current in FW mode is reduced due to increasing FW current and phase impedance, resulting in reduced torque as speed increases, as indicated in Figure 1. To achieve higher output power with the same motor, one possible solution is to use serial windings at low speed and then reconfigure the serial windings to parallel windings at high speed. In Figure 1(b), the torque and power characteristics versus speed of an IPMSM with serial (solid lines) and parallel windings (dotted lines) are depicted qualitatively. With parallel windings, the motor's back-emf is halved and the FW control is used at a higher speed, which roughly increases the constant torque range by 100% and therefore peak is also increased by about 100%. In the meantime, the peak torque with parallel windings is also roughly halved; the phase inductance of the parallel windings is one fourth of the serial winding phase inductance. When the motor is at low speeds, serial windings are selected to achieve high torque output, and parallel mode is selected to achieve higher power at high speeds. This two-speed range drive will have better torque-speed (T-ω) and power-speed (P-ω) characteristics than a one-speed range motor drive. This can be particularly useful for alternative motor technologies without RE materials, as they tend to have lower power densities than that of RE PM machines. Reconfigurable winding solutions were developed to reduce motor size for a given power rating, increase motor output power for a given size, and improve system drive cycle efficiency. Impacts on system volume/cost and advantages of changing torque-speed characteristics compared with mechanical hydraulic transmissions and their peripheral components were considered during these developments.

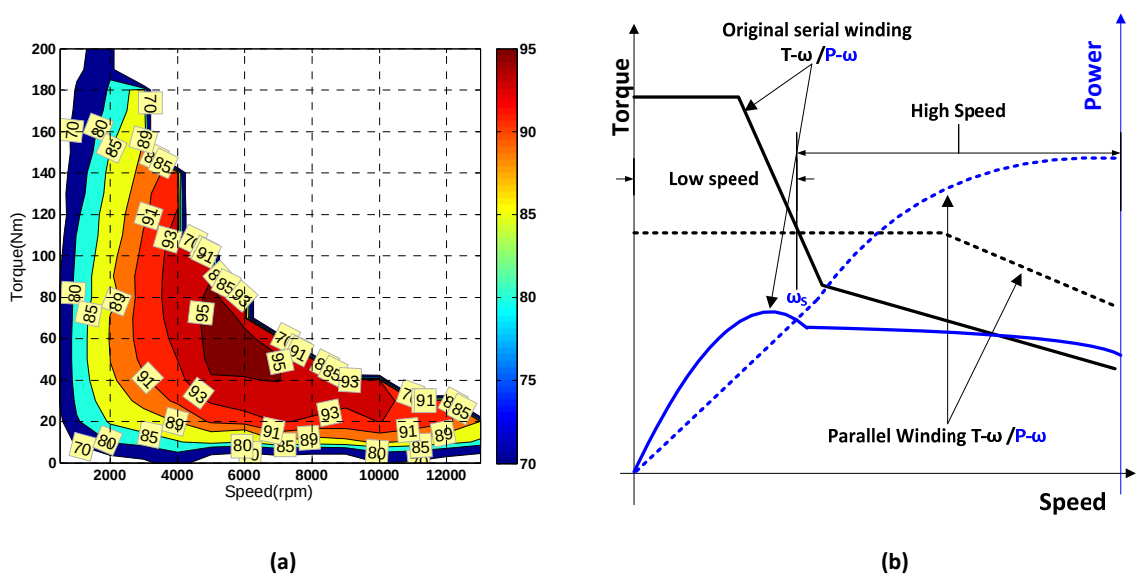


Figure 1: Efficiency contour of an IPMSM drive used in a commercial HEV (a) and comparison of characteristics of original serial and parallel windings of the drive (b).

Results and Discussion

Review of Previous Work

Reconfigurable windings, also known as switchable windings, have already been implemented in electric motors, and some products are already on the market. For example, some three-phase induction motors use a star-delta soft-starter to reduce the inrush current when they start and operate with a fixed 60 Hz frequency. A star winding is initially selected, which has a larger impedance and back-emf; then when the motor builds up its speed and back-emf, it switches to a delta winding arrangement so that it can go to higher speed/higher power operation. Recently, more papers/patents have reported progress on reconfigurable windings approaches for automotive applications. For example, Eckart and Erik worked on reconfigurable windings for a surface-mounted PM synchronous motor and published several papers in the 1990s [2]. Chen and Cheng, by using relays, developed a motor with reconfigurable windings for electrical transmission applications and with brushless dc motors to expand the speed range [3–4]. Huang and Chang developed reconfigurable windings in an induction motor to achieve faster motor start-up [5]. Hsu, Fulton, Krieger, and Shum filed different patents recently for reconfigurable winding motors [6–8]. This approach uses ac switches to change the configuration of the windings so that the motor operating mode can be changed to achieve a wider speed range and faster motor starting. Another approach uses pole-changing motors to achieve expanded operation. Most methods under this approach are suitable only for induction motors.

Figure 2 illustrates two important industry patents on this topic. Figure 2(a) is a diagram representing patent A, for a system in which eight ac switches are used to change the star-connected stator windings between parallel and serial connections. In parallel mode, the five blue ac switches are on and the three orange switches are off; in serial mode, the five blue switches are off and the three orange switches are on. Figure 2(b) (patent B) represents a system patented in 2012 for electric bike applications. It uses only three ac switches rather than eight, which is a great improvement over patent A. In parallel mode, K_{P1} and K_{P2} are on and K_S is off; in serial mode, K_S is on and K_{P1} and K_{P2} are off. However, this system must use two small inverters instead of one. Further, note that all three switches must be installed in a dc bus; that arrangement may increase the total dc bus stray inductance, which will in turn increase the voltage spikes on the dc bus. This makes it less suitable for high-power applications. Note also that patent B has a dc short-circuit failure mode if all three switches are on at the same time, and some extra protection should be considered.

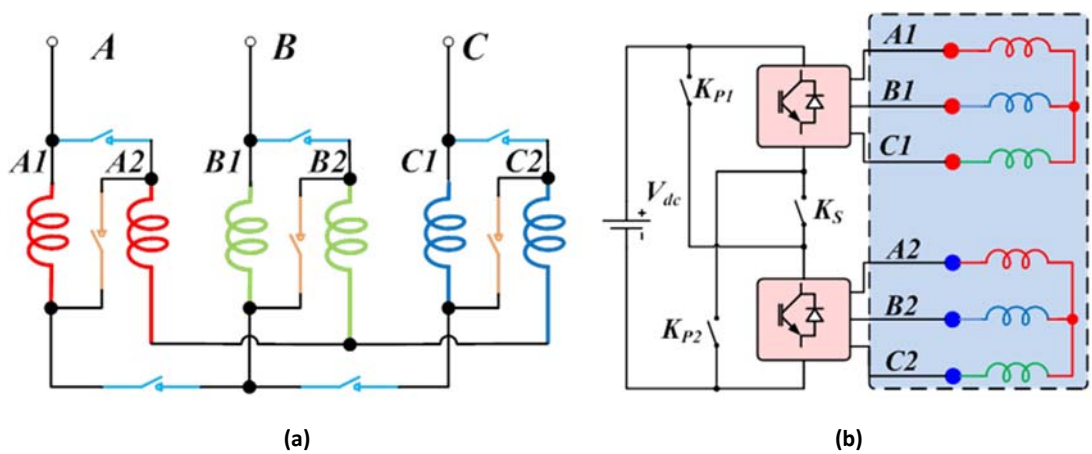


Figure 2: Schematics illustrating two industry patents: (a) Patent 20110234139 A1 (published in 2011 by Hsu) and (b) patent B-US20120086380 (published in 2012 by Krieger and Shum).

Proposed Designs

A new reconfigurable windings design was proposed to achieve expanded operation; the overall block diagram can be seen in Figure 3. Compared with the patent A approach shown in Figure 2, the proposed design uses fewer ac power switches, and because it does not insert ac power switches in the dc bus, it does not have the dc short-circuit failure mode that patent B has. To evaluate the advantages, the inverter losses of the design proposed in patent A were compared with those of the new approach, with the loss model including both

switching and conduction losses. The basic equations used to calculate switching loss and conduction loss in a three-phase voltage source inverter can be seen in Eqs. (1)–(3). Equation (1) shows the inverter switching loss, where f_{SW} is the switching frequency, V_{dc} is the dc bus voltage, I_{PEAK} is the peak phase current, V_{ref} and I_{ref} are the voltage and current at which the switching losses are given, E_{ON_IGBT}, E_{OFF_IGBT} are the turn-on, turn-off loss of the insulated gate bipolar transistor (IGBT), and E_{OFF_DIODE} is the turn-off loss of the diode.

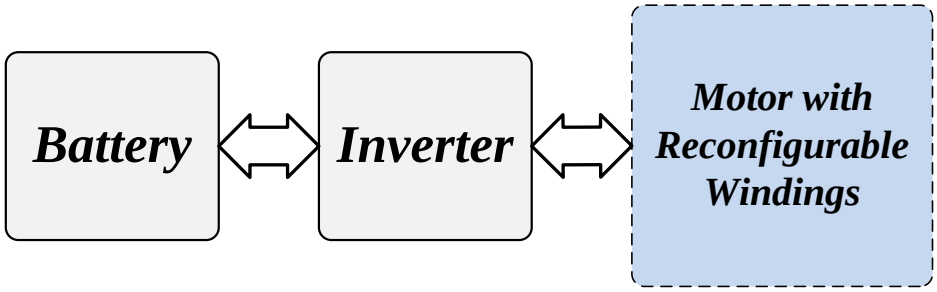


Figure 3: Proposed reconfigurable windings approach.

Equation (2) shows the conduction losses of the IGBT, in which V_{CEO} and r_{IGBT} are the zero current saturation voltage and equivalent resistance of the IGBT, m is the modulation index, and θ is the power displacement factor. Equation (3) shows the conduction losses of the diodes, in which V_{fO} and r_d are the zero current forward voltage and equivalent resistance of the diode. The voltage source inverter total loss can be calculated using Eqs. (1)–(3). The losses associated with the solid-state ac switches for changing windings configurations are also considered in Eq. (4), where V_{CER0} is zero current forward voltage drop and r_R is the equivalent resistance of the solid-state ac switch (relay). The key parameters of an off-the-shelf IGBT module with a 1,200 V/450 A rating were used in the simulation. A switching frequency of 7.5 kHz was used with a 650 Vdc bus voltage, and the motor peak phase current was 250 A.

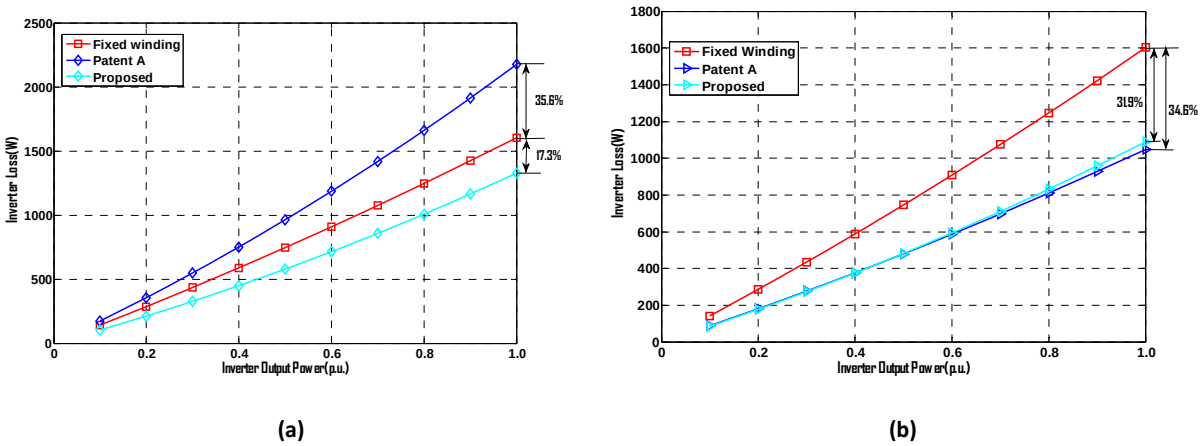
$$P_{SL} = \frac{6 f_{sw} V_{dc} I_{Peak}}{\pi V_{ref} I_{ref}} \times \left(E_{ON_IGBT} + E_{OFF_IGBT} + E_{OFF_DIODE}\right) \tag{1}$$

$$P_{CL_IGBT} = I_{PEAK} V_{CEO} \left(\frac{1}{2\pi} + \frac{1}{8} m cos\theta\right) + I_{PEAK}^2 r_{IGBT} \left(\frac{1}{8} + \frac{1}{3\pi} m cos\theta\right) \tag{2}$$

$$P_{CL_D} = I_{PEAK} V_{f0} \left(\frac{1}{2\pi} - \frac{1}{8} m cos\theta\right) + I_{PEAK}^2 r_d \left(\frac{1}{8} - \frac{1}{3\pi} m cos\theta\right) \tag{3}$$

$$P_{CL_R} = I_{PEAK} \left(\frac{2V_{CER0}}{\pi} + \frac{I_{PEAK}^2 r_R}{2}\right) \tag{4}$$

Figure 4 shows the total inverter losses of different approaches. The trace with red squares shows the inverter loss of a fixed windings motor at different peak phase currents from 50 A up to 250 A. The trace with blue diamonds shows the loss of the patent A design at high speed; the trace with cyan diamonds shows the loss of the proposed reconfigurable windings approach at high speed. The trace with blue triangles shows the loss of the patent A design in low speed; the trace with cyan triangles shows the loss of the proposed reconfigurable winding approach at low speed. It can be seen that the patent A design has the highest loss, while the fixed winding motor has the second highest loss. It is clear that the proposed reconfigurable winding approach has lower losses in both low-speed and high-speed operation compared with the fixed winding motor. For high speeds, the loss reduction is 17.3%, and for low speeds, it can be as high as 31.9%. Compared with the patent A approach, the proposed reconfigurable windings approach achieves a significant loss reduction of about 40% at high speed. Note that the loss at low speed is slightly higher (+2.7%) than that of the patent A approach. The results show the proposed reconfigurable windings approach can reduce power loss much more than the approach proposed in patent A.



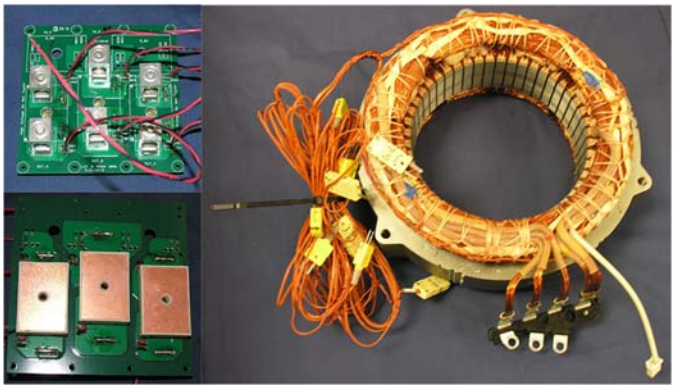
(a) (b)

Figure 4: Simulated losses for the proposed design, fixed windings, and patent A system at high speed (a) and low speed (b).

Design of Low-Cost ac Switch Circuit and Benchtop Component Test of Switching Transients

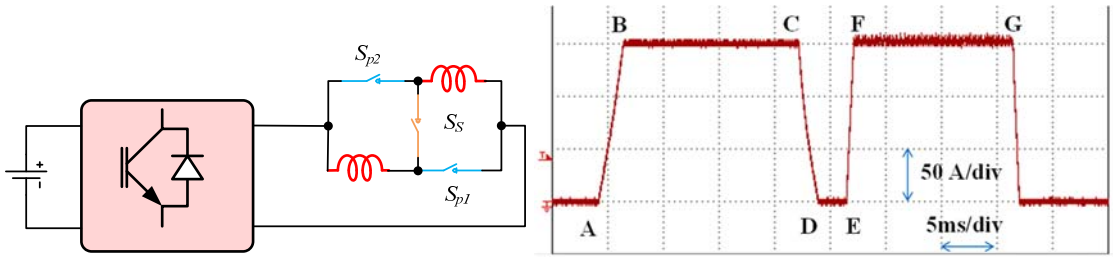
As the winding configuration is changed, the drive will experience some switching transients, which must be considered with respect to switch selection and potential torque pulsations in vehicle propulsion. During the first transient, the controller firstly needs to bring all the phase currents down to zero. Secondly, the ac switches will turn on/off to change the windings' configuration. Finally, the controller will build up the three-phase currents to the new operating point. Because all three-phase currents are zero in switching transient, there is a torque interruption in the powertrain, which is not desirable. The duration of torque interruption is determined by the speed of the ac switches. If fast solid-state ac switches are used, each turn on/turn off takes only about 1–2 ms; the torque interruption time could be shorter than 10 ms. However, if slow ac switches like ac contactors are used, the undesirable torque interruption could be longer. Further, the ac contactors have limited operating cycles because of the mechanical parts. All these drawbacks make the ac contactor unattractive for automotive applications. To minimize the torque interruption, fast and low-cost solid-state ac switches were selected in this project.

A 4.2 by 4.3 in. printed circuit board (PCB) was designed to switch the motor three-phase windings as indicated in Figure 5(a). Anti-parallel thyristor modules were used as the ac switches. There are some off-the-shelf, solid-state ac switches on the market. However, they are fairly expensive—around $100 for a switch with a 660 V/125 Arms rating. An anti-parallel thyristor module with a similar rating costs only about $15 (for quantity >1,680). It also has a smaller footprint than the off-the-shelf solid-state ac switches. An HEV motor with three-phase windings was used in the test. To simulate a switch winding transient, the windings were rearranged between series and parallel configurations. A single-phase inverter controlled by a digital signal processor was used for the real-time test. Figure 5 shows the ac switch PCB assembly and the motor winding. At top left is the top view of the PCB and at bottom left is the bottom view. Three solid-state ac switches were installed. Figure 5(b) is the motor, which was used in a commercial HEV drive system. Figure 6(a) shows the test diagram. The windings configuration can be changed between parallel and serial connection by turning the three ac switches on and off. Figure 6(b) shows the test waveform. The waveform shows the inverter output current in a transient from series mode (A-B-C-D) to parallel (E-F-G). The ac switches change the configuration of the windings between points D and E. The inverter current ramp-up/ramp-down time during the transient is about 2.45 ms (1.75 ms from C to D and 0.7 ms from E to F), and the total transient is only 5.0 ms. Because the serial windings configuration has higher inductance, it takes a longer time to ramp up/ramp down the current than it does in parallel mode. A dc bus voltage of 100 V was used in the test. Note that the current ramp-up/ramp-down time will be much faster with typical hybrid bus voltages in the range of 300–700 Vdc. The test results show the designed ac switch PCB assembly can change the motor windings configuration in a fairly short time. Research continues to be done to further reduce the transient.



(a) (b)

Figure 5: Solid-state ac switch board [(a) top, PCB top view; (a) bottom, PCB bottom view) and (b) motor windings used in benchtop test.



(a) (b)

Figure 6: Test circuit diagram with an inverter and three solid-state ac switches (a) and key test waveform of a series to parallel transient, output current 50 A/div, time 5 ms/div (b).

Design Strategies for Reducing PM Volume in EV Traction Drives using Reconfigurable Windings

Design strategies were developed for the use of reconfigurable windings to improve the performance of interior PM (IPM) machines while reducing the amount of PM materials consumed. An electric machine with a reconfigurable winding can be defined as any electric drive system which is able to change, by means of electronic switches, between two or more impedance modes as viewed at the machine terminals. Most of the literature on reconfigurable winding machines is for either induction machines or surface-mounted PM (SMPM) machines. Particularly, the goal of most of these investigations is to increase the constant power speed range (CPSR) of the machine.

One of the first reported reconfigurable winding devices was an induction motor for spindle applications requiring a wide CPSR. The authors reportedly achieved a CPSR of 1 : 12 using a delta–to–wye reconfiguration. The system successfully replaced a mechanical gearbox in a lathe cutting test. Another winding commutation approach for induction machines used two coil groups to effectively change the number of machine poles. Similar techniques exist for switching both the pole and phase configuration and the pole and turn configuration. Switched winding induction machines have also been investigated specifically in the context of EV applications.

Changing the stator windings by altering the number of turns is a strategy suitable for both induction and PM machines. For PM machines, it is possible to achieve a field weakening effect by putting a center tap in the phase coils and operating them in series or parallel. It is also possible to use a delta–to–wye changeover configuration with additional center taps for each phase, allowing four different modes of operation. A technique for switching between the three natural winding configurations—star, pentagon, and pentacle—for a five–phase PM machine was also explored.

There has been little investigation into IPM machines with reconfigurable windings. This may in part be due to the fact that IPM machines can be well designed with a wide CPSR. However, achieving a wide CPSR in this way imposes a trade-off between low speed torque, high speed power, and the relative balance of PM and reluctance torque. This trade-off is closely tied to the relationship between the rated and characteristic currents of the machine.

A significant difference between IPM topologies and the others previously investigated is the presence of reluctance torque. To achieve the high saliency ratio required for a large reluctance torque, there must be an easily saturable magnetic flux path in the machine. The nonlinear nature of magnetic saturation makes it difficult to study the effects of changes in the winding configuration using simple models. In these studies, numerical simulations of a simple IPM topology were used to examine the trade-offs that exist between torque and power density.

A simple design strategy for a machine that has windings reconfigurable between a series and parallel mode begins with designing the series configuration to maximize the torque produced by the machine while constraining the characteristic current to be equal to half the rated current. From there, increased power—both maximum and continuous—can be achieved above the series mode base speed by switching to the parallel winding configuration. Our studies show that by using a switched winding approach, it is possible to obtain torque and power versus speed characteristics similar to that of a standard IPM machine with a significant decrease in PM material.

Theory for Design of IPM Machine with Reconfigurable Winding

The fundamental equation for torque production of an IPM machine in the rotor D–Q reference frame is given by

$$\tau = \frac{3P}{4}\left[\lambda_{pm} I cos(\theta) + \frac{1}{2}\left[L_q - L_d\right] I^2 sin(2\theta)\right] \ , \tag{5}$$

where I is the stator current amplitude, $\theta$is the stator current angle, L_d and L_q are, respectively, the direct– and quadrature–axis inductance, λ_{pm} is the PM flux--linkage (aligned with the direct axis), and P is the number of machine poles. The direct-- and quadrature--axis currents are given by $I_d = Isin(\theta)$ and $I_q = Icos(\theta)$.

The fundamental voltage equations for an IPM machine, ignoring the stator resistance, in the rotor D-Q reference frame is given by

$$V_d = \omega_e L_q I cos(\theta) \tag{6}$$

and

$$V_q = \omega_e(\lambda_{pm} - L_d I sin(\theta)) \ , \tag{7}$$

where $V_d$and V_q are the direct and quadrature axis voltages with voltage magnitude $V = \sqrt{V_d^2 + V_q^2}$ and ω_e as the electrical frequency in radians per second. An important quantity of interest for IPM machines is the characteristic current, obtained by setting $V_q = 0$, which is the ratio of the permanent flux–linkage to direct-axis inductance, $I_c = \frac{\lambda_{pm}}{L_d}$. The characteristic current is the direct–axis current amplitude required to completely cancel the PM flux linkage coupled to the stator, resulting in zero quadrature voltage. The characteristic current can be more generally defined as satisfying the equation $L_d(I_c, 0) = \lambda_{pm}$ for nonlinear magnetic models, where the direct-axis inductance $L_d(I_d, I_q)$ is a function of I_d and I_q. Finally, there will be some operational limitations placed on the machine as a result of the inverter rating. We assume $I \leq I_r$ and $V \leq V_r$, where I_r is the rated current and V_r is the rated voltage.

For sufficiently high rated speeds, machines with $I_c > I_r$ cannot produce constant power over their entire speed range because they are not capable of full field weakening. Machines with $I_c < I_r$ are capable of full field weakening and can deliver constant power over a wide speed range. However, this power is generally less

than the peak power over all speeds because the maximum current amplitude must decrease due to voltage limitations at higher speeds.

The torque equation reveals that around the maximum torque operating point, τ is about constant with respect to θ. Where $\tau = 0$ at $\theta = 90°$, τ varies about linearly with θ. Therefore, at worst, the torque is linearly decreasing as θ is adjusted for field weakening. When a significant amount of reluctance torque is available, τ will vary like I^2 at high torque levels and like I at low torque levels. The analysis for the voltage magnitude V is more complicated, but it can be estimated that the voltage varies linearly with both θ and I at any operating point. This means that if the current amplitude must be decreased because of voltage limitations and large inductances, the torque will decrease faster with I than the speed will be allowed to increase. This will result in reduced power output above the base speed of the machine.

A perfectly flat constant power speed range can be obtained by designs where $I_c = I_r$. These designs have peak constant power capabilities greater than the peak power delivered at the base speed due to the fact that τ is constant with respect to θ at the maximum torque operating point. Achieving the $I_c = I_r$ characteristic for a given peak torque requirement implies a precise relationship between the required torque, PM flux, direct–axis inductance, and saliency ratio. Under these constraints, the only method of reducing the amount of PM material is to increase the saliency ratio.

For a fixed saliency ratio, it is possible to decrease the amount of PM material while maintaining the same peak torque level by uniformly increasing L_d and L_q by, for example, increasing the number of turns in the stator or increasing the diameter of the stator bore. This, however, will decrease I_c and lead to a reduction in the peak power for the reasons previously discussed. A different way to state this is that for a given peak torque level, machines that more closely match the requirement that $I_c = I_r$ will tend to have higher power capabilities in the constant power region. This is demonstrated with two design examples below.

For an IPM machine with a reconfigurable winding structure and $I_c = I_r$ in series mode, switching to a parallel winding configuration does nothing to improve the performance of the drive. This decreases the peak torque and field-weakening capability by increasing the characteristic current to $I_c \approx 2I_r$. This also introduces a dangerous short circuit fault mode if the drive is not capable of handling twice the rated current.

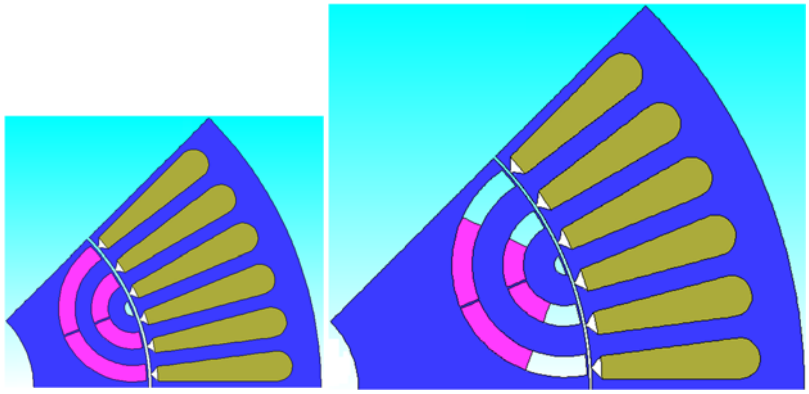
The situation is different for an IPM machine design with, for example, $I_c = 0.5I_r$. In this case, switching from a series to a parallel winding configuration will still decrease the peak torque, but the field-weakening capability in this mode will be improved because $I_c \approx I_r$ in parallel mode. That is to say, the peak torque in the parallel mode will be deliverable at higher speeds than the same torque in the series mode. Moreover, the peak power in the constant power speed range in the parallel configuration will be flat above the base speed as there will be no need to decrease the current amplitude. Therefore, it is possible to think of the series winding configuration as a low speed/high torque mode, and the parallel configuration as a high speed/high power mode.

It is also possible to approach the design problem as requiring $I_c = I_r$ in parallel mode and view switching into a series mode as a method of increasing the peak torque capability. However, this would imply that significant headroom exists in the magnetic circuit to allow doubling the number of amp turns without too much saturation occurring. It is likely that existing designs with $I_c = I_r$ are already aggressively sized to maximize power and torque with respect to saturation of the magnetic circuit. When approaching a design from scratch with the intent of using a reconfigurable winding, either may be viable. The difference is whether the problem is approached as one of optimizing peak torque capability with the constraint that $I_c = 0.5I_r$ or peak power capability with the constraint that $I_c = I_r$.

Design Examples

To illustrate the trade-offs that can be made in achieving similar design goals in machines with and without reconfigurable windings, a coarse optimization of two machines was performed with different stack lengths, l_s, and stator outer radii, r_{si}, but fixed active volume given as $\pi r_{is}^2 l_s$ and maximum peak current density as 8 A-RMS. The inverter constraints were assumed to be 290 A peak per phase with a dc-link voltage of 375 V. The two resulting designs are shown in Figure 7. The base case machine has $l_s = 150$ mm, $r_{si} = 100$ mm, and very nearly matches the requirement that $I_c = I_r$ after being optimized to maximize the peak torque

capability. The basic parameters for the optimization procedure were the stator bore, stator tooth thickness, and magnet thickness.



(a) (b)

Figure 7: Comparison of two different machine designs with different ratio of characteristic current to rated current: (a) machine design with stack length of 150 mm, stator outer radius of 100 mm, and $I_c \approx I_r$; (b) machine design with stack length of 75 mm, stator outer radius of 141 mm, and $I_c \approx 0.5I_r$.

The machine intended for use with reconfigurable windings was designed in two stages. First, the aspect ratio was changed so that $l_s = 75$ mm, $r_{si} = 141$ mm so that the active volume is the same as the base machine. Second, the machine was optimized over the same parameters as the base machine to maximize the torque output. The resulting torque is greater because the larger stator outer radius is able to accommodate more turns. Last, the arc length of the magnets was reduced to give the same peak torque capability as the base case machine. The reconfigurable winding machine ends up having the same peak torque capability as the base case machine with about 40% less PM material.

The torque–speed curves associated with both machines are given in Figures 8 and 9. The peak torque capabilities of the base machine and the reconfigurable-winding machine (in series mode) are both about 320 Nm. The base machine has a base speed of about 2,500 rpm. In series mode, the reconfigurable winding machine has a base speed of 2,000 rpm and in parallel mode 4,500 rpm—more than double. Additionally, the peak torque available in parallel mode is 190 Nm, which is greater than 50% of the series mode torque and much more than predicted by the linear torque model. This is an important but subtle point: saturation occurring in series mode means that switching to a parallel winding configuration will typically increase the power delivered at the new base speed. This is in contrast with reconfigurable winding schemes previously reported for SMPM machines, which have essentially the same power at base speed regardless of the winding configuration. That is, the linear model is more accurate for SMPM than for IPM machines.

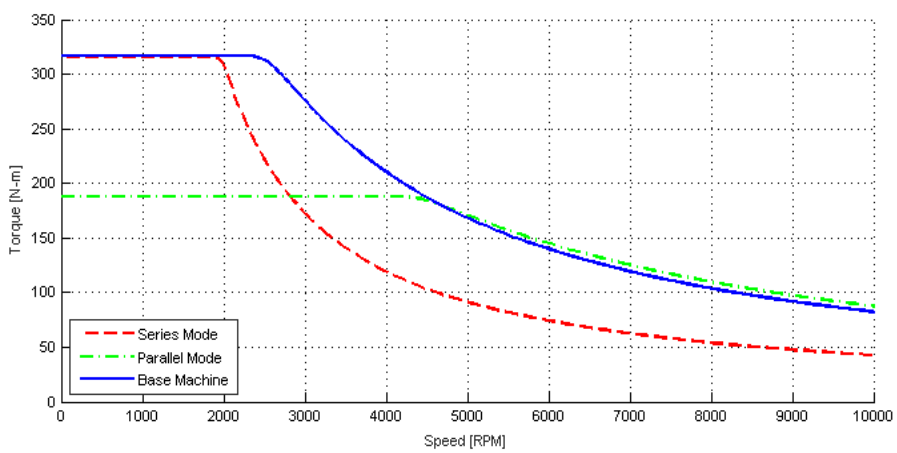


Figure 8: Torque-speed curve demonstrating the performance of both machines.

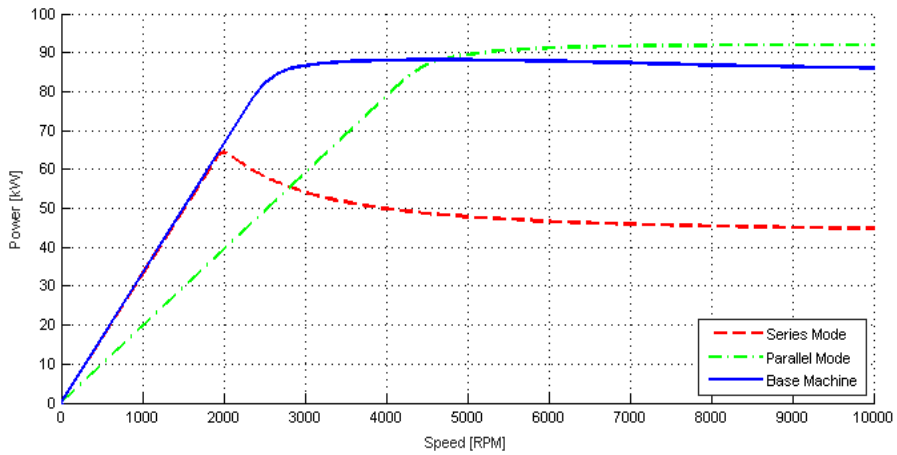


Figure 9: Power-speed curve demonstrating the performance of both machines.

The relationship between the rated current, characteristic current, and peak power capability is most easily understood by examining the power-speed curves. The base case machine has $I_c \approx I_r$ and a flat peak power above the base speed. Moreover, the power at the base speed is about 81 kW, while the peak power available from 3,000 rpm up to the maximum speed is greater than 85 kW.

The situation for the series-mode reconfigurable winding machine is different. In this mode, the machine has $I_c \approx I_r$ and a corresponding local maximum in the power-speed curve. The peak power at the base speed is 65 kW, which decreases to 45 kW as the machine approaches its maximum speed. Switching to a parallel mode allows us to achieve a peak power capability similar to the base machine's, with 89 kW available at the base speed, approaching 92 kW as the speed increases to 10 krpm. This is more than double the series-mode case.

It should be noted that the procedure used to arrive at this design does not necessarily minimize the PM material under the constraint that the peak torque capabilities be the same as those for the base case machine. This comprehensive optimization was beyond the scope of this study. Additionally, in comparing the torque- and power-speed curves of base and reconfigurable winding machines it can be seen that there are some drawbacks to the reconfigurable winding machine. In particular, there is a region on the torque-speed plane that is reachable by the base machine but not by the reconfigurable winding machine. It is unlikely that it is possible to design a reconfigurable winding machine that has exactly the same torque-speed characteristic as a standard machine. The nonconforming regions are an important design trade-off that must be considered. In this instance, it was mitigated by reducing the PM volume to give the same peak torque capability. Another valid approach would be to choose the design so that the torque-speed curves of the base and the series-mode reconfigurable machine intersect at a given point (e.g., the base speed). This approach may still reduce the total PM volume—although to a lesser extent—but increase the performance of the machine.

The impact of reconfigurable winding on motor efficiency was studied using a PM motor similar to that of the Prius. Efficiency maps for both modes of operation were generated. A combined efficiency map is shown in Figure 10, with serial and parallel operational areas indicated. For this plot, the highest efficiency was selected for each torque-speed operation point. It can be observed that the parallel mode greatly expands the high efficiency regions for high power operation points. Using the same data, a differential efficiency plot, shown in Figure 11, was created by subtracting serial mode efficiencies from parallel mode efficiencies. It should be noted that for clarity this map only illustrates differential efficiency in areas that overlap. It can be seen that low speed, high torque efficiencies can be up to 10% higher in serial mode, whereas high speed, low torque efficiencies can be up to 10% higher in parallel mode.

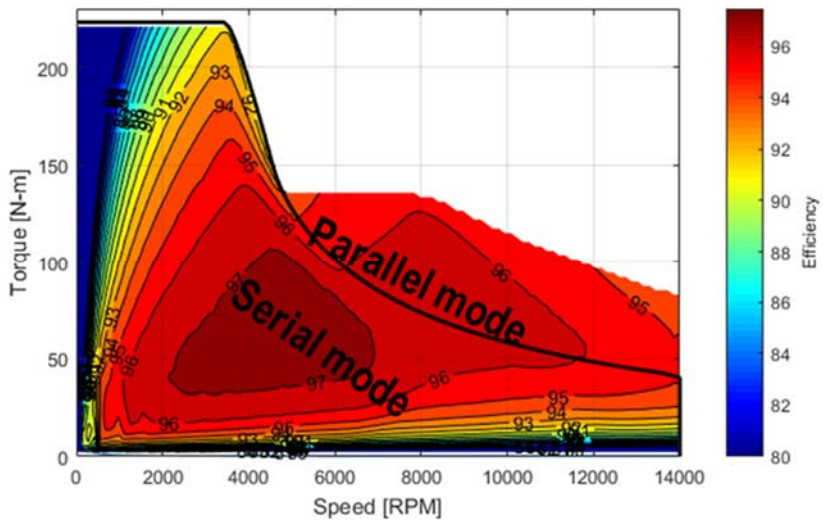


Figure 10: Combined efficiency plot for serial and parallel modes.

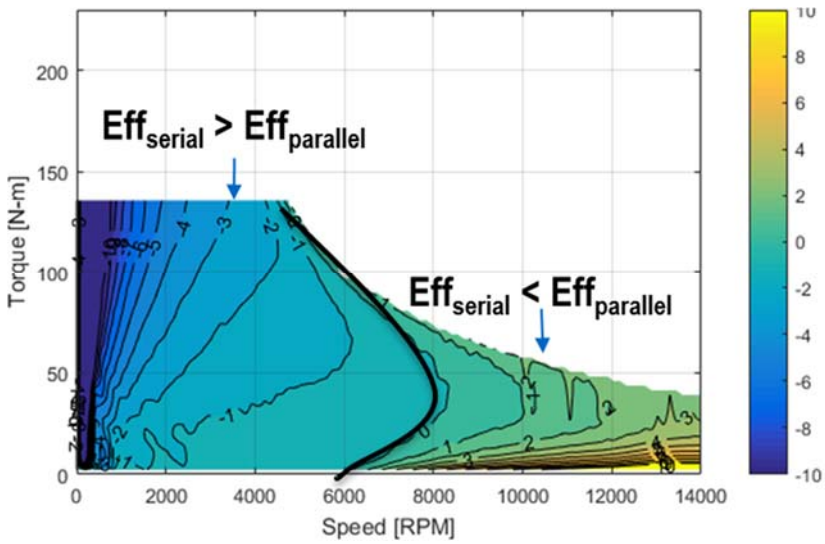


Figure 11: Differential efficiency plot for serial and parallel modes.

Conclusions and Future Directions

Several reconfigurable winding approaches were developed that have fewer solid-state switches and eliminate battery short-circuit failure modes. Fewer solid-state switches facilitate a reconfigurable winding solution with low cost and high switching efficiency. A low-cost solid-state switch circuit and PCB was designed, fabricated, and tested to demonstrate that acceptable switching times could be achieved. Initial test results show that reconfiguration can be achieved in about 5 ms. Future work will include a cost study with consideration of reduced motor size and additional component and material costs and comparisons with mechanical gearboxes.

From a motor design perspective, theoretical investigations were performed to understand when IPM machines can benefit from the use of reconfigurable windings. It was found that machines with characteristic currents equal to about half their rated currents can achieve much higher power operation at high speeds by changing from series to parallel mode. This effectively doubles the characteristic current and allows for field weakening to occur in the high speed region without having to reduce the current vector magnitude.

An exemplar design process was performed to illustrate one potential trade-off that can be made between machines with and without reconfigurable windings. First, a base case machine was developed with equal characteristic and rated currents. Second, a series-mode reconfigurable winding machine was designed to meet the torque capability of the base case machine with half the characteristic current and less PM material. Comparisons of the torque-speed and power-speed profiles of the two machines indicate they have similar performance characteristics, with the base case machine outperforming the reconfigurable winding machine only in a small region around its base speed. In addition to demonstrating performance improvements, this study shows that considerable efficiency improvements can be realized with a reconfigurable winding approach.

FY 2016 Presentations/Publications/Patents

1. T. Burress et al, "Multi-speed range electric motor R&D," presented at the DOE Vehicle Technologies Program Electric Drive Technologies Electrical and Electronics Technical Team meeting, December 2015, Southfield, Michigan.
2. L. Tang et al, "Electric motor performance improvement techniques," presented at the DOE Vehicle Technologies Office 2016 Annual Merit Review, June 2016, Washington, DC.

References

1. T. A. Burress, "Evaluation of the 2010 Toyota Prius Hybrid Synergy Drive System," available at http://info.ornl.gov/sites/publications/files/Pub26762.pdf.
2. E. Nipp, "Alternative to field-weakening of surface-mounted permanent-magnet motors for variable-speed drives," in *Proceedings of the IEEE Industry Applications Society Annual Meeting*, **1**, pp.191–198, 1995.
3. C.-H Chen and M. Y. Cheng, "Design of a multispeed winding for a brushless dc motor and its sensorless control," *Electric Power Applications, IEE Proceedings*, **153**(6), pp. 834–841, November 2006.
4. Cheng-Hu Chen, Ming-Yang Cheng, and Ming-Shun Tsai, "Study on a wide speed range integrated electrical transmission system," *Power Electronics and Drives Systems, 2005 (PEDS 2005. International Conference)*, **1**, pp.781–786, 2005.
5. H. Huang and L. Chang, "Electrical two-speed propulsion by motor winding switching and its control strategies for electric vehicles," *IEEE Transactions on Vehicular Technology*, **48**(2), pp. 607–618, March 1999.
6. John Hsu, "Electronically commutated serial-parallel switching for motor windings," US Patent 20110234139 A1, published September 29, 2011.
7. D. A. Fulton, "Switch module for an electric machine having switchable stator windings," US Patent 8415910 B2, published April 9, 2013; also published as US 20120068656 A1, March 22, 2012.
8. M. Krieger and H. Shum, "Electric motor having windings operable in parallel and/or series, and related methods," US Patent 20120086380 A1, published April 12, 2012.

3.1 Electric Drive Wide Bandgap Power Electronics

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Contract No.: DE-AC05-00OR22725

Abstract/Executive Summary

The overall objective of this project is to design and develop a high-voltage–wide bandgap (WBG) 30 kW continuous, 55 kW peak power traction drive system including a dc-dc boost converter and a three-phase inverter. This project is targeted toward the application of WBG technology and novel circuit topologies with advanced packaging to address inverter cost, weight, volume, and efficiency goals. Specific research and development efforts in FY 2016 include new WBG device evaluation consisting of short circuit capability test and failure mechanism analysis; gate driver and protection function improvement for high-reliability, high-frequency, high-density boost converter design with advanced substrate layout and packaging techniques; and high-density three-phase inverter design. The new concepts developed under this project will increase the power density and decrease the volume and weight for electric vehicle traction-drive inverters and will achieve the DOE 2022 weight, volume, and efficiency targets.

Accomplishments

- Completed static and dynamic evaluation of a 600 V trench-type silicon carbide (SiC) metal oxide semiconductor field-effect transistor (MOSFET) and a 900 V SiC double-implanted MOSFET (DMOSFET).
- Completed short circuit capability evaluation and post-failure analysis of 600 V trench-type SiC MOSFET.
- Completed module and heat sink design of a 30 kW WBG-based boost converter prototype using ORNL's WBG modules.
- Completed design, build, and test of a gate driver with improved short circuit protection function.
- Completed system level layout design of a 30 kW WBG-based liquid-cooled inverter.

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Introduction

The need for high-temperature operation of power electronics in automotive applications is increasing. The ability of components to operate reliably at elevated temperatures can enable cost and weight savings by making it feasible to reduce the sizes of heat sinks and eliminate secondary cooling loops. Additionally, devices capable of increased-frequency operation can reduce requirements for passive components, leading to

further reductions in cost, weight, and volume. WBG devices, specifically SiC and gallium nitride (GaN) semiconductors, are emerging technologies that enable operation at higher temperatures and frequencies with efficiency and reliability improvements. The development of WBG devices promises to help achieve cost, weight, and volume goals, as well as DOE Vehicle Technologies Office targets. WBG technology assessment performed under this project will help determine when a viable market introduction of these devices for automotive use will occur. The independent assessment of devices for the automotive industry is carried out to monitor progress and provide data readily when the need arises.

None of the electric drive vehicle traction drive systems on the market can meet cost and efficiency goals. Efficiency is achieved by using lower loss devices and materials, which tend to be expensive, even as quantity levels increase. A case in point is motor lamination steel, the lower loss grades of which are manufactured using novel processes that add more cost.

Problems associated with power electronics for advanced vehicle applications include the following.

1. Low efficiency at light load conditions for inverters and converters
2. Low current density and device scaling issues for high-power converters
3. Lack of reliable higher junction temperature devices
4. High cost of devices and power modules, especially for WBG and advanced silicon devices
5. High number of components for low-voltage electronics (e.g., gate drivers, controllers, sensors)
6. Lack of standardized high-power-density, low-cost power modules for scalable and modular power converters
7. Substrates that use expensive ceramics for thermal stability and reliability
8. Low-cost, low-loss magnetics and high-temperature films for capacitors

The goal of this research is to reduce the size and weight of power converters to meet the 2022 DOE inverter targets. The overall strategy for addressing the limitations of the state of the art is shown in Figure 1.

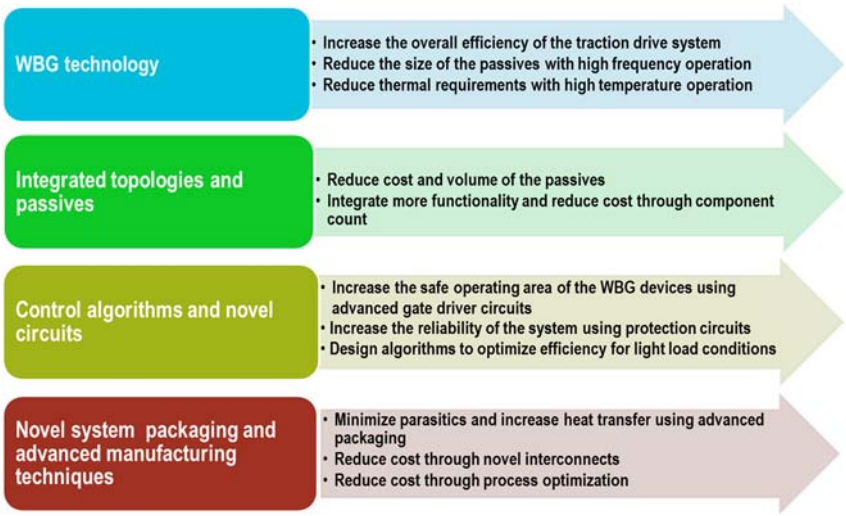


Figure 1: Overall strategy to address limitations of the state of the art.

Approach

The overall objective of this project is to design and develop a WBG 30 kW continuous and 55 kW peak power inverter. WBG devices offer some distinct advantages over their silicon components. Primarily, they can operate at higher junction temperatures. This benefit allows for hotter coolant and smaller heat sinks and can potentially facilitate air cooling without sacrificing performance. Many of the components in a typical commercial inverter cannot withstand the desired operating temperature of WBG devices (e.g., the capacitor

and gate driver). Thus, the inverter as a whole must be considered in the development of new high-temperature packages.

The design innovations in this project include the following.

1. The design concept uses layers of high-temperature thermal insulating material to separate the low-temperature components from the high-temperature zone.
2. The design uses the high-temperature operating capability of WBG devices to enable air cooling and uses newer fast-switching SiC devices for high-temperature-liquid designs.
3. The heat sink design minimizes thermal resistance.
4. The design is optimized for the most frequently operated points.

These new concepts will increase the power density and decrease the volume and weight for electric-based vehicle traction-drive inverters and will achieve the DOE 2022 weight, volume, and efficiency targets. The specific approach to address the limitations of the state of the art is described in Figure 2.

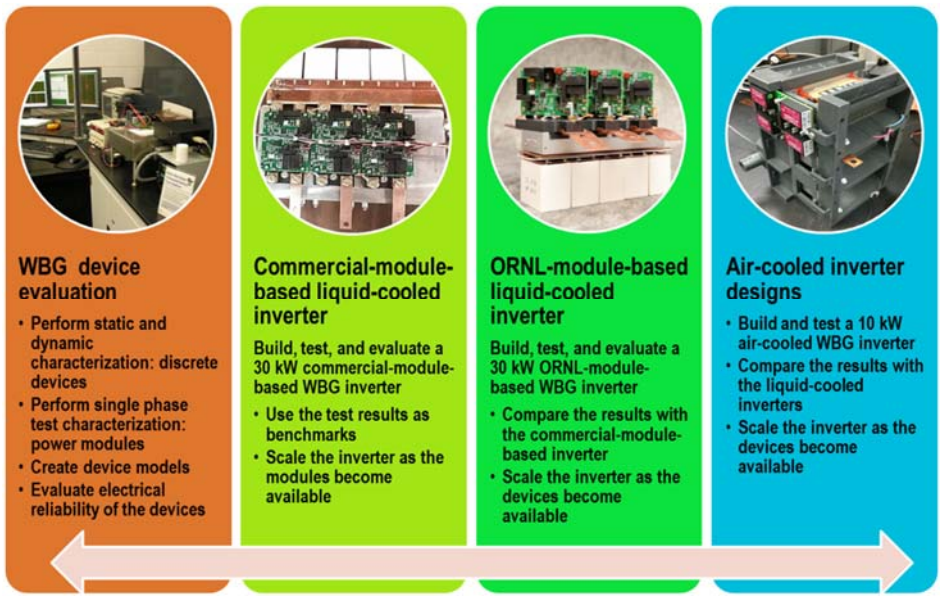


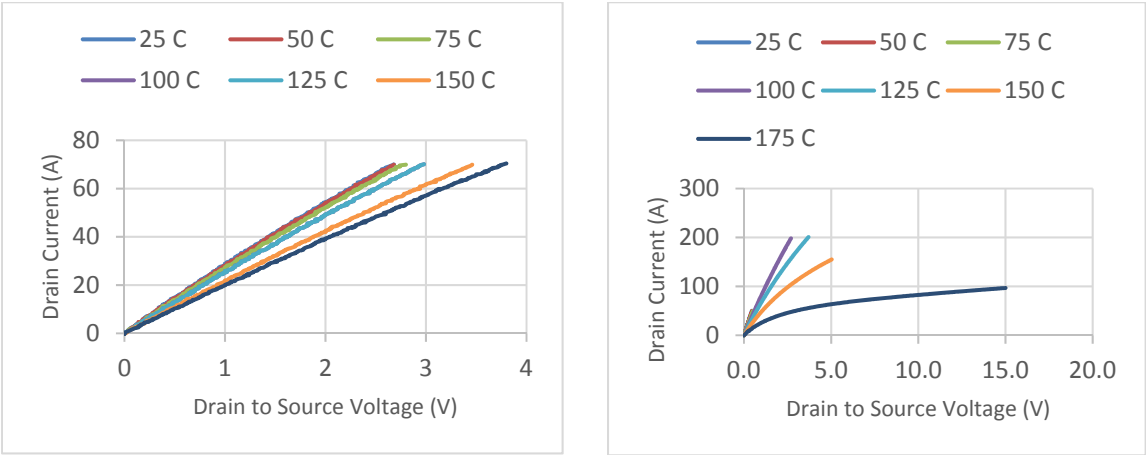
Figure 2: Specific approach to address limitations of the state of the art.

Results and Discussion

1. Device Testing

1.1 Static Characterization

The new WBG devices acquired this year are 650 V trench-type SiC MOSFET samples and 900 V SiC DMOSFET samples. On-state characteristics and switching energy losses of the devices were obtained over a wide temperature range. All the devices obtained were experimental samples. Static characterization, including output characteristics, body diode characteristics, third quadrant characteristics, and device capacitances, has been conducted for both devices. Due to space limitations, only the temperature-dependent output characteristics are included in this report, as shown in Figure 3.



(a) (b)

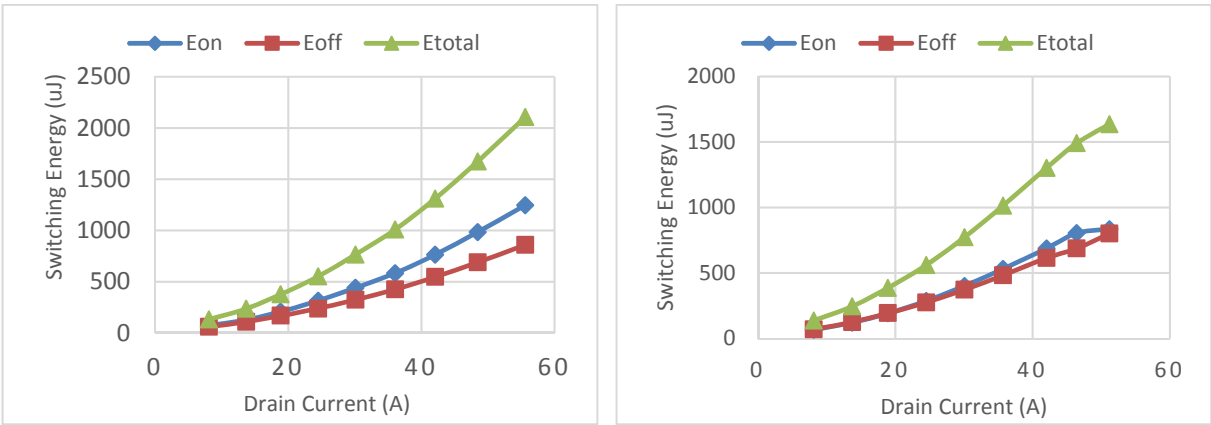
Figure 3: Temperature-dependent output characteristics of 600 V trench-type SiC MOSFETs (a) and 900 V SiC DMOSFETs (b).

The dynamic performance of both kinds of SiC MOSFETs is characterized by the "ORNL Wide Bandgap Device Evaluation Facility." Specifically, a universal double pulse power test setup is used to test their switching performance. The test setup has several advanced features such as (1) built-in solid-state circuit breaker for overcurrent and short circuit protection, (2) compatibility with silicon/WBG devices featuring various device packages (TO-220, TO-247, etc.), and (3) compatibility with different measurement methods (shunt, Pearson, current probe).

To maintain the consistency of the test, the same freewheeling diode (FWD), gate resistance, and gate voltage are used. A CREE C3D10170H is used as FWD. The inductance, gate resistance, and applied gate voltage parameters are as follows: 148 µH, 5 Ohm, and -2/+20 V. The gate driver used for this testing was a commercial gate driver chip with high-sourcing and high-sinking current capability.

1.2 Dynamic Characterization

The turn-on and turn-off switching energies for the 650 V trench MOSFETs at 400 V are shown in Figure 4, under 25°C and 175°C case temperatures. The switching energy for temperature variation is also plotted in Figure 5. The turn-on switching energy decreases with the increase of temperature while the turn-off energy increases with the increase of temperature.



(a) (b)

Figure 4: Turn-on and turn-off switching energies for a 650 V trench-type SiC MOSFET at 25°C and 400 V (a) and at 175°C and 400 V (b).

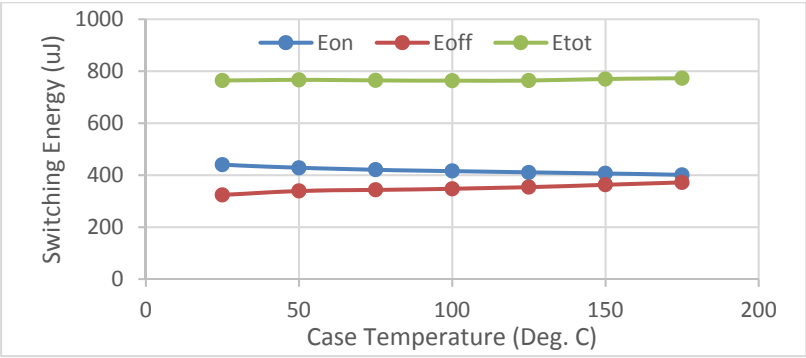
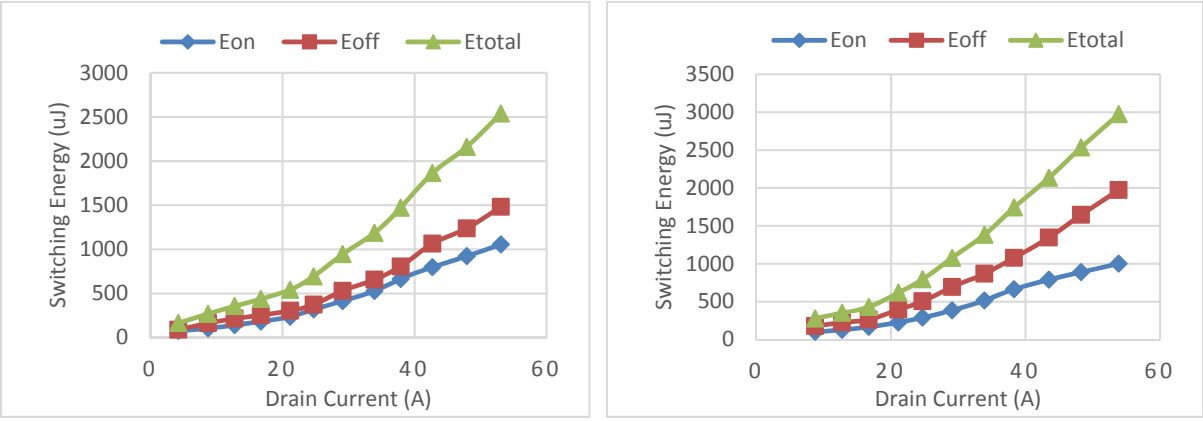


Figure 5: Switching energy as a function of temperature for a 650 V trench-type SiC MOSFET at 400 V.

The trench MOSFETs exhibit much lower total switching energy compared to DMOSFETs tested in previous years. Compared to the 1200 V trench SiC MOSFET tested in FY 2015, the trench MOSFET tested in FY 2016 provides higher switching energy. The main reason is that the 600 V trench device has much higher input capacitance.

The turn-on and turn-off switching energy for the 900 V SiC DMOSFET at 600 V dc bus voltage is shown in Figure 6 under case temperatures of 25°C and 175°C. The switching energy at 600 V bus voltage for temperature variation is also plotted in Figure 7. The turn-on switching energy reduces with the increase of temperature while the turn-off energy is increased with the increase of temperature.



(a) **(b)**

Figure 6: Turn-on and turn-off switching energies for a 900 V SiC DMOSFET at 25°C and 600 V (a) and 175°C and 600 V (b).

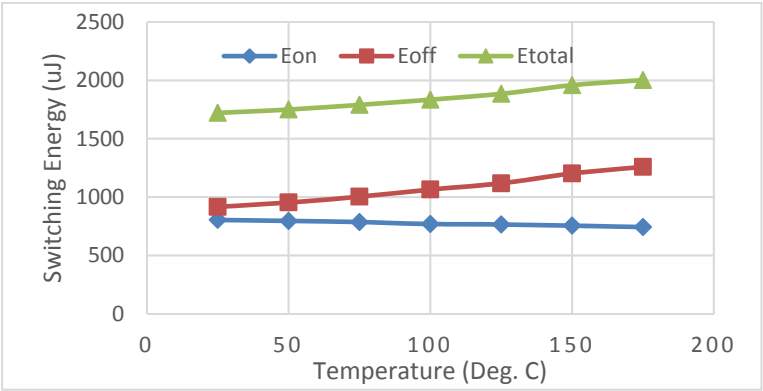
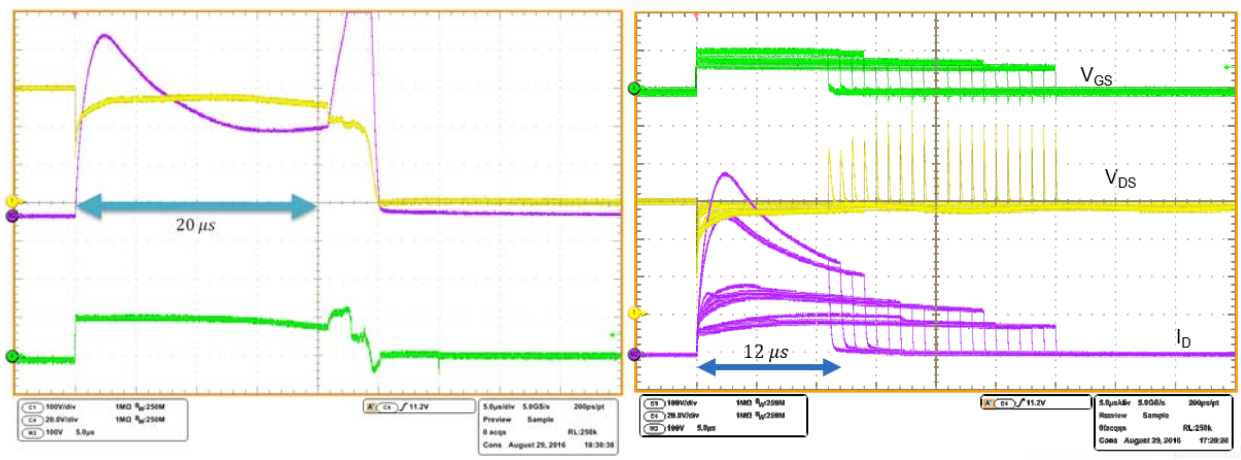


Figure 7: Switching energy as a function of temperature for a 900 V SiC DMOSFET at 600 V.

1.3 Short Circuit Test

The short circuit test provides a good understanding of device operation with the design of the protection circuit. Due to limited available research samples, the short circuit test is only conducted on 650 V trench SiC MOSFETs. The test setup is similar to the setup published in [1], [2]. The turn-off gate resistance is increased to 25 Ω to prevent avalanche failures caused by turn-off voltage spikes. The gate voltage is kept at the same level -2/+20 V (turn-off/turn-on). Because it is a 650 V trench device, the short circuit test is conducted with a dc bus of 300 V. For real usage realization, the short circuit test is conducted at 75°C and 100°C case temperatures.

During the short circuit test, two sets of short circuit tests are considered—protected and unprotected short circuit tests. The protected short circuit test is the scenario where the protection circuit can turn off the gate signal. The unprotected short circuit test is the scenario where the protection is not applied. The unprotected short circuit test is shown in Figure 8(a). The device withstands the short circuit current for about 20 µs. After 21 µs, thermal runaway is observed, which leads to very high current until the current is cut by a solid state dc circuit breaker.



(a) (b)

Figure 8: Short circuit test at 100°C with unprotected mode (a) and protected mode (b).

In the protected short circuit test [Figure 8(b)], the device is short circuited using a controlled gate pulse. The gate signal is gradually increased from 1 µs to 30 µs. The device presents consistent short circuit behavior before 12 µs, with a peak current of 470 A. With a short circuit pulse of 13 µs, the current peak value decreases to 380 A, and the saturation current also decreases. The possible reason is that the electron mobility of the device decreases with the increase of junction temperature. After 14 µs, the device degrades further and the bulk resistance increases. This phenomenon leads to further reduction of short circuit current. After 24 µs, the short circuit current is clamped to around 100 A.

The test provides a very interesting example of the short circuit tolerance of the trench device. After the short circuit, the degraded devices show significantly increased drain-source impedance. This increased impedance effectively reduces the short circuit current, regardless of increased short circuit pulses. No delayed thermal runaway is observed during the gradual increase of the protective short circuit pulse. After conducting the short circuit test, the devices are labeled and saved for post-failure analysis. In the post-failure analysis, the damaged or degraded devices will be compared with a good device.

After conducting the short circuit test for both 75°C and 100°C for both protected and unprotected failure, static characteristics analysis is conducted to characterize the property changes of the device and get some idea of the damage that occurs for trench MOSFETs under these conditions. The post-failure analysis is performed at 25°C.

The output characteristic comparison in Figure 9(a) shows significant increase in the device on-resistance and when 20 V gate voltage is applied. The significant on-resistance increase indicates an open-circuit-like

behavior of the devices. The output characteristics are also checked at 0 V for all the damaged devices. No current flow is observed for this condition. This is a fairly positive finding as it indicates the device did not cause a short path even after failure.

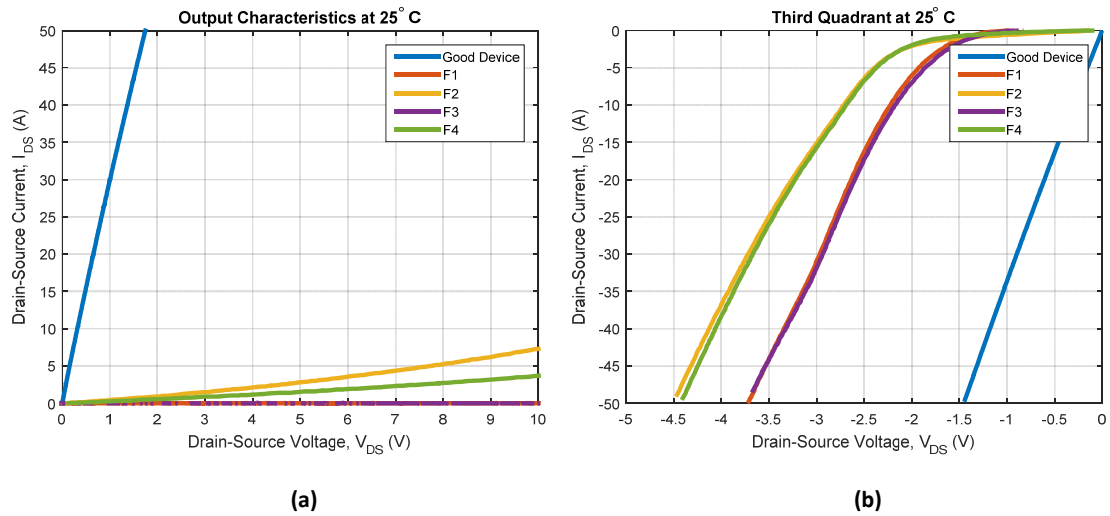


Figure 9: Comparison among failed devices: output characteristics (a) and third quadrant characteristics (b). F1 = protected short circuit test conducted at 75°C, F2 = unprotected short circuit test conducted at 75°C, F3 = protected short circuit test conducted at 100°C, and F4 = unprotected short circuit test conducted at 100°C.

The third quadrant characteristic indicates that the channel conduction has been significantly impacted. For the F1 and F3 samples, the gate has a small amount of control, a very small current is flowing through the channel, and most of the current is flowing through the body diode. For F2 and F4, which suffered unprotected short circuit failure, the channel conduction has been lost and the body diode conducts all the current.

2. Gate Drive/Protection Improvement

A two-channel gate drive board has been designed based on the available commercial gate drive chips for the SiC power module. In the design of the gate driver, in addition to meeting the basic driving requirements of SiC MOSFETs (e.g., sourcing and sinking current, positive/negative voltage level, power consumption), several key issues associated with the high switching speed of SiC devices are considered. First, an auxiliary circuit is designed to suppress the crosstalk phenomenon for the phase-leg module, and the switching power loss can be reduced with less or no cross-conduction between the upper and lower side switches. Second, a soft turn-off circuit is used to safely cut off short circuit current without causing avalanche breakdown.

In the layout design, the gate driving loops are minimized to lower the gate loop inductance, thus reducing gate voltage oscillations during fast switching transients. The power copper plane and signal copper plane are designed to be well separated so that the induced printed circuit board parasitic capacitance, degrading switching performance, can be eliminated.

Another key improvement on the gate driver is the flexible shut down mode for desaturation protection, as shown in Figure 10. For the adopted commercial SiC MOSFET gate driver, there is no permanent shut down function, and the maximum fault output holding time of the chip is around 200 ms. Users must rely on the central controller to permanently shut down the converter, which is not reliable under strong electromagnetic interference and solid fault conditions. To address this issue, an auxiliary control circuit is added to realize local shut down. (The circuits involved will be discussed in detail in a future publication.)

Figure 11 illustrates the protection mode of the desaturation function without and with the auxiliary control circuit. As can be seen from the testing results, when the desaturation protection function is triggered, the pulse width modulation (PWM) signal is blocked for around 200 ms. However, after the holding duration, the PWM signal is reactivated automatically. For a solid short circuit condition, this protection mode causes periodic short circuit current and protection activation for semiconductor devices, and eventually the devices will be degraded and damaged due to thermal fatigue. With the developed auxiliary control circuit, gate drive can be

shut down locally (i.e., holding fault status permanently), as shown in Figure 11(b). Any short circuit fault condition in the inverter will be detected, and semiconductor devices and inverters will be protected locally, without notifying the central digital controller.

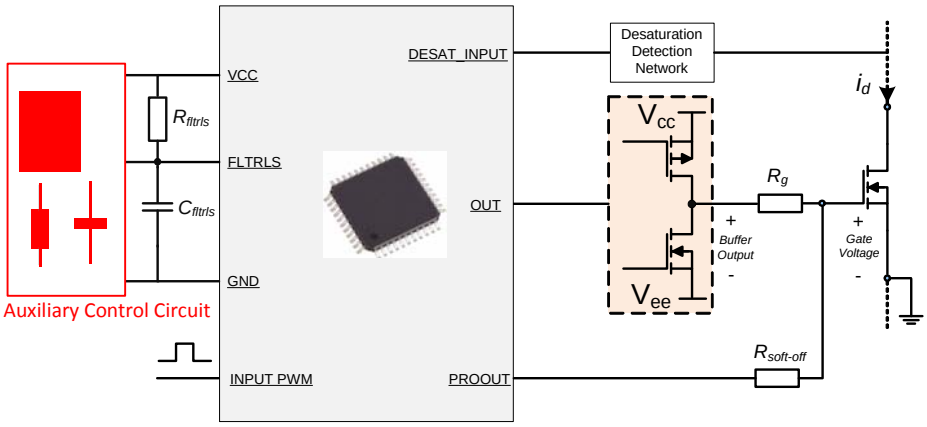
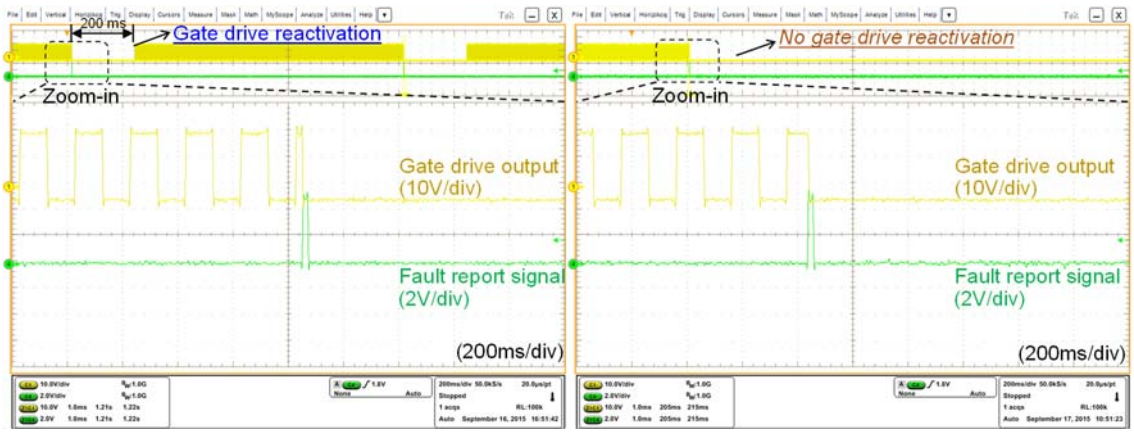


Figure 10: Commercial gate drive chip with auxiliary control circuit.



(a) (b)

Figure 11: Desaturation protection mode without auxiliary control circuit (a) and with auxiliary control circuit (b).

3. WBG Inverter Design and Development

Device packages able to withstand high temperatures are required to take advantage of the high-temperature operating capability of WBG devices. Various organizations are working on high-temperature packaging for high-temperature devices. Several high-temperature packages, which include discrete device packages for power modules, have been reported in the past several years. Novel packaging concepts focus primarily on improving the existing packages or on designing new packages using new materials and or processing techniques for better reliability and performance. Even though the novel packages enable the devices to work at higher temperatures, theoretical advantages such as the current density of WBG devices are not realized because of the limitations of the interconnects needed for the power module to access the device terminals. In addition, the novel device packages need further development to be used in full systems.

Other factors that prevent system designers from reaping the benefits of WBG technology are the low-voltage electronics and the passive components. This is because even though the packages and the power devices can handle high temperatures, the low-power electronics that drive the power devices, silicon-on-insulator (SOI)–based technologies, are limited to a maximum temperature of 200°C. Silicon-based electronics are limited to 125°C operating temperatures. Although SOI-based electronics can work at up to 200°C, they are expensive. High-temperature (over 200°C) electronics have been reported as being feasible; however, as they have not

been built, their performance capabilities are still in question. It could be many years before a logic-level high-temperature transistor can be built. This time lag creates a void in the power module industry, especially for intelligent power module products, which include the electronics inside the module.

Similarly, the passive components in an inverter have lower operating temperatures and cannot be operated in close proximity to high-temperature WBG devices. This situation leads to an increase in the volume and a reduction in the power density of the system. High-temperature passive components are currently being developed to address the high-temperature-operation requirement. However, as with the electronic components, they will be much more expensive than the low-temperature components.

To address these problems, a system-level approach for packaging design needs to be developed. Complex 3-dimensional (3-D) packaging structures with integrated interconnects can reduce the required assembly steps and increase the power densities of power electronic systems. Recent advancements in additive manufacturing (AM) promise an exciting future, with WBG technology making inroads in the power electronics industry. AM techniques enable the development of complex 3-D geometries that will result in size and volume reductions at the system level by integrating low-temperature components with high-temperature active devices and reducing the material needed to build the heat exchangers in inverters. ORNL has developed expertise in AM in the last few years. ORNL's Power Electronics and Electric Machinery team recognized the potential of this technology for power electronics system packaging and took the first step toward achieving a completely printed inverter concept.

A 10 kW all-SiC inverter incorporating an aluminum-based printed power module with an integrated cooling system and a printed plastic lead frame was built using AM techniques. By leveraging previous research achievements, this project aims at the design and development of a high-power (>30 kW), high-frequency (>50 kHz) boost converter to meet the 2022 power density target. To develop the boost converter, high-frequency, high-density WBG power modules capable of high switching speeds need to be designed as a first step. To meet this requirement, a 1200 V, 200 A, all-SiC module, discussed in the following sections, is being designed.

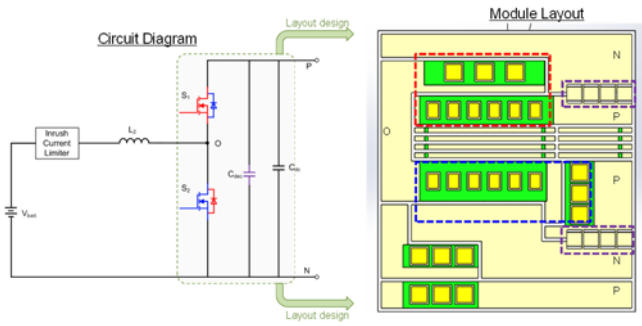
3.1 Power Module

The phase-leg power module uses research samples of trench SiC MOSFETs and commercial SiC Schottky diodes. To reach the rated current, six MOSFETs and three diodes are paralleled in each switch position. Figure 12 shows the circuit schematic and layout design of the power module.

The phase-leg power module is built on a single substrate soldered onto the flow channel. The aluminum flow channel is electrically insulated from the positive (P terminal) and negative (N terminal) dc bus by the aluminum nitride substrate. The phase trace (O terminal) of the direct-bonded copper (DBC) is connected to the external inductor, as seen in the mechanical layout diagram. In the design of the DBC layout, the following key considerations are taken into account.

1. All semiconductor devices are integrated into one substrate, and decoupling capacitances are embedded for small switching commutation loop, and thus low-power loop, parasitic inductances. Also, the embedded decoupling capacitances can potentially help to suppress electromagnetic noise issues during continuous operation.
2. The "P-cell–N-cell" concept [3] is adopted to minimize the power loop parasitic inductance for high-frequency operation. The switching commutation loops between high-side MOSFETs and low-side diodes, and high-side diodes and low-side MOSFETs, are the main targets to be shrunk.
3. Lossy devices (i.e., lower MOSFETs) are located in the center of the module to improve thermal performance.

The power loop parasitic inductances and current distribution of the designed substrates are obtained through finite element analysis (FEA) simulation using the ANSYS Q3D Extractor. According to the simulation results, the lumped parasitic inductance is 4.11 nH for the high-side MOSFET and low-side diode commutation loop and 3.44 nH for the high-side diode and low-side MOSFET loop, as shown in Figure 13. Moreover, current is evenly distributed within both switching loop areas, as shown in Figure 14.



(a) (b)

Figure 12: Boost converter diagram (a) and DBC layout design of the power module (b).

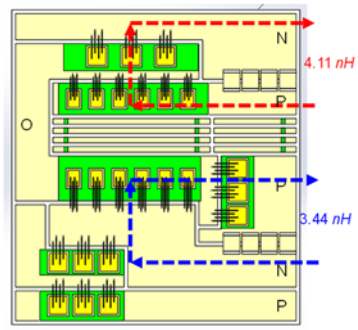
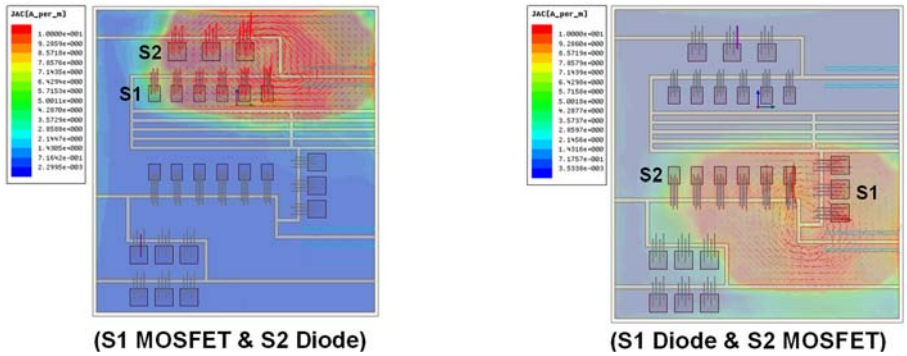


Figure 13: Power loop parasitic inductance of the boost module.



(a) (b)

Figure 14: Current distribution of the boost module: S1 MOSFET and S2 diode (a) and S1 diode and S2 MOSFET (b).

3.2 Heat Sink

A genetic algorithm (GA) –based approach is applied for designing heat sinks based on total heat generation and dissipation for a prespecified size and shape. This approach combines random iteration processes and GAs with FEA to design the optimized heat sink. With an approach that favors "survival of the fittest," an optimal heat sink can be designed uniquely for this particular boost converter.

For the boost converter heat sink design, four main steps are included: initialization, evaluation and selection, crossover and mutation, and reproduction. The initialized population is implemented by the random walking process. In a nutshell, with a predefined inlet and outlet position, one branch of channels is created by separate steps, with random direction and random step distance, under predefined constraints. Multiple branches of channels together become an individual. As a corresponding, the direction and distance data are the chromosome, the FEA heat sink geometry in COMSOL is the character, and the evaluated maximum junction temperature by the right-hand side COMSOL simulation process is the fitness value. Based on individual chromosome and fitness values, better ones have higher survival possibility, and as a result, the optimal result

will evolve itself iteration by iteration. Eventually, after certain iterations, the best result can converge as shown in Figure 15.

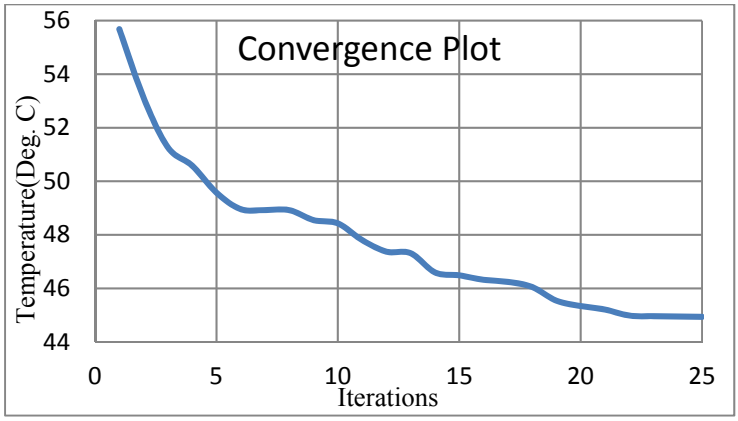
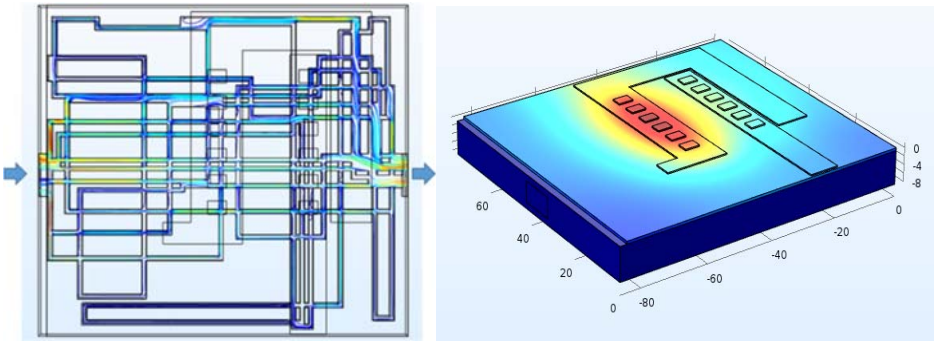


Figure 15: Convergence plot of the heat sink optimization.

The final optimized heat sink with the streamline plot and the temperature map of the heat sink with the designed power module are shown in Figure 16. According to the simulation results, the maximum junction temperature is about 103°C and the overall heat sink volume is 86 mm × 77 mm × 8 mm, which is about 53,000 mm³; the total weight is about 120 g.

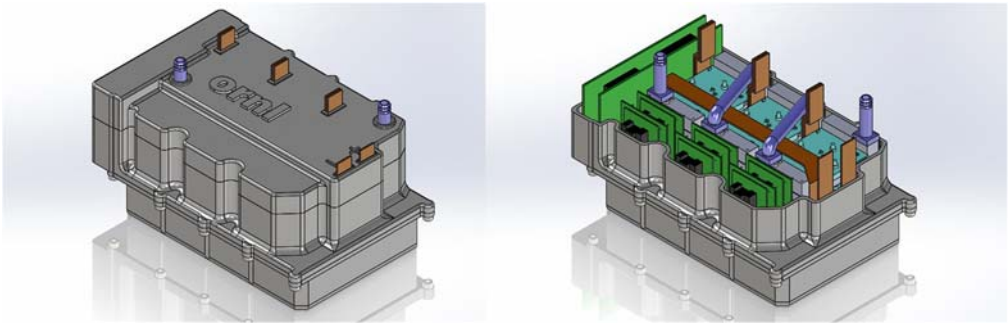


(a) (b)

Figure 16: Simulation results for the optimized heat sink: streamline plot (a) and temperature distribution (b).

3.3 Inverter Layout

A 30 kW all-SiC three-phase inverter is also under development using commercially available 1200 V SiC MOSFET modules. The layout of the inverter is shown in Figure 17.



(a) (b)

Figure 17: Conceptual 3-D drawing of the 30 kW three-phase liquid-cooled inverter: overview (a) and uncovered view (b).

Commercially available gate drivers from Rohm will be used. The performance of the power module will be evaluated before the inverter is built. The modules are mounted on the cold plate, with thermal grease as the heat transfer medium, from the lower side of the power modules. This prototype model will be packaged as shown in Figure 17, with controls and capacitors packaged close to the heat sink. The capacitors used in this design are not a brick type but small individual capacitors in series to ensure better cooling and reduced costs. The key advanced features of this new design include lower convection thermal resistance by using a new optimized 3-D–printed cold plate, higher power density compared to the previous 30 kW liquid-cooled inverter, and modular design (wire-bond module, cold plate, bus bars, etc.) for easy fabrication.

Conclusions and Future Directions

The electric drive inverter R&D activities in FY 2016 include performance evaluation of the latest WBG devices; gate drive and protection function improvement; and high-frequency, high-density boost converter and three-phase inverter design. The WBG device evaluation results, including static, dynamic, and short circuit characterization, provide realistic data for design of reliable high-density inverters. The improvement in protection function further ensures robust operation of the WBG inverters under development. The innovative power module design results in low-switching commutation loop inductance, enabling full exploitation of WBG power device capabilities such as fast switching speed. In addition, the heat sink optimization based on GA has resulted in reducing thermal impedance. The benefits gained from these innovations can lead to high-efficiency, high-density system operation beyond the limits of state-of-the-art technologies.

WBG device evaluation will continue until the technology is transitioned to industry. The innovative technologies used in FY 2016 design work will be demonstrated to show the improvement in power density and reliability. The testing results will also show that WBG technology will aid in achieving U.S. DRIVE targets for volume, efficiency, power density, and system costs.

FY 2016 Presentations/Publications/Patents

1. Zhiqiang Wang, Madhu Chinthavali, and Steven Campbell, "Characterization and comparison of planar and trench silicon carbide (SiC) power MOSFETs," *ECS Transactions*, PRiME 2016/230th ECS Meeting, accepted for publication in October 2016.
2. Madhu Chinthavali, "Additive manufacturing technology for power electronics applications," presented at the industry sessions on 3D Power Packaging, IEEE Applied Power Electronics Conference and Exposition, March 2016, Long Beach, California.
3. Madhu Chinthavali, "Electric drive inverter R&D," presented at the 2016 DOE Vehicle Technologies Office Annual Merit Review, June 2016, Washington, DC.
4. Madhu Chinthavali, "Future of semiconductor technology development," presented at the 2016 DOE Vehicle Technologies–EDT Industry Engagement Meeting, August 2016, Knoxville, Tennessee.

References

1. Z. Wang, X. Shi, Y. Xue, L. M. Tolbert, F. Wang, and B. J. Blalock, "Design and performance evaluation of overcurrent protection schemes for silicon carbide (SiC) power MOSFETs," *IEEE Transactions on Industrial Electronics*, **61**(10), pp. 5570–5581, October 2014.
2. Z. Wang et al., "Temperature-dependent short-circuit capability of silicon carbide power MOSFETs," *IEEE Transactions on Power Electronics*, **31**(2), pp. 1555–1566, February 2016.
3. S. Li, L. M. Tolbert, F. Wang, and F. Peng, "Stray inductance reduction of commutation loop in the P-cell- and N-cell-based IGBT phase-leg module," *IEEE Transactions on Power Electronics*, **29**(7), pp. 3616–3624, July 2014.

3.2 Wide Bandgap Converters and Chargers

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Contract No.: DE-AC05-00OR22725

Abstract/Executive Summary

- The overall objective of this project is to develop low-cost, high-efficiency, high-power-density all–wide bandgap (WBG) dc-dc converters and onboard chargers (OBCs). The goal is to reduce charger converter cost by 50% and weight and volume by a factor of 2 compared with the state of the art and to provide charger efficiency of more than 96%.
- A major objective for FY 2016 was to develop a gallium nitride (GaN)–based charger dc-dc converter. A compact, lightweight, highly efficient, 6.6 kW isolated three-port charger converter was designed and built using the latest GaN Systems GaN transistors; a three-dimensional (3-D) printed cold plate; high-voltage (HV) heavy copper printed circuit board (PCB) power planes; low-voltage (14 V), high-current PCB power planes; and a planar transformer. The prototype has a power density of 10.5 kW/L and specific power of 9.6 kW/kg. The volume and weight were reduced, respectively, to 47% and 21% of that of a silicon (Si) –based counterpart. Testing and characterization of the prototype was successfully completed, with the results showing greater efficiency than the Si-based counterpart, even at 2.5 times the switching frequency.
- Another objective for FY 2016 was to integrate the GaN charger converter with a silicon carbide (SiC) traction drive system to test and characterize the functionality as an OBC at the level 2 charging power of 6.6 kW. To this end, the isolated GaN charger dc-dc was integrated with a 100 kW segmented traction inverter that uses commercial SiC metal oxide semiconductor field-effect transistors (MOSFETs) and 3-D printed components. Testing and evaluation of the integral onboard charging functionality was successfully completed at power levels up to 6.6 kW.
- Test results on magnetic cores that were three dimensionally printed using nanocomposite magnetic powders revealed issues with the current printing process and possible future work to address these issues was identified.

Accomplishments

- Completed design for a 6.6 kW charger converter using the latest GaN transistors manufactured by GaN Systems Inc.; a 3-D-printed cold plate; HV heavy copper PCB power planes; low-voltage (14 V), high-current PCB power planes; and a planar transformer. Completed building and testing a prototype with a power density of 10.5 kW/L and specific power of 9.6 kW/kg. Comparing the prototype to a Si-based counterpart, the GaN-based converter achieved the following:

- 50% reduction in volume,
- 75% reduction in weight, and
- peak efficiency of 99% vs. 98.4 % for the Si-based counterpart (even at a 2.5 times higher switching frequency).

- Successfully tested an integrated OBC using the 6.6 kW GaN charger converter and a 100 kW segmented traction drive system that was built using SiC MOSFETs. An improvement of 2.2 percentage points in charger system efficiency over a Si-based counterpart was observed.
- Completed testing and evaluation of magnetic cores that were 3-D printed at ORNL's additive manufacturing facility using nanocomposite magnetic powders produced by Aegis Technology Inc. Test results indicated very low core losses but a small relative permeability of 2. Future work needs to focus on increasing the relative permeability by reducing the air gaps in the cores.

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Introduction

Most plug-in electric vehicles (EVs) and battery EVs on the market use a stand-alone OBC to charge the HV traction battery packs. However, a stand-alone OBC is not cost-effective because of its large number of components. Moreover, its performance in terms of weight, volume, and efficiency is limited by the operating frequency capabilities of existing Si-based semiconductor and magnetic materials. Bulky and expensive passive components, including inductors, capacitors, and transformers, are needed in OBCs because of low switching frequencies with Si switches (< 100 kHz) at power levels of several kilowatts and low saturation flux densities (~0.3 T) and high core losses at high frequencies with soft ferrite magnetic materials. As a result, OBCs (1) add significant cost (~$106/kW), (2) have low power-density and specific-power numbers (~0.6 kW/kg, ~0.8 kW/L), (3) are relatively inefficient (85–93%), and (4) are unidirectional (i.e., can charge the battery but are incapable of vehicle-to-grid support, a highly desirable function in future smart grids).

The problems and limitations of existing Si-based OBC technology are addressed in this multiyear project by using WBG devices, advanced magnetic materials, and novel integrated charger topologies and control strategies to significantly increase power density, specific power, and efficiency at lower cost. Emerging WBG devices—including those made with SiC and GaN—and advanced soft magnetic materials enable significant improvements in ac-dc and dc-dc converters, major components of OBCs. Their ability to operate with reduced conduction and switching losses over higher frequencies and temperatures minimizes requirements for the passive components and reduces cooling demands. In addition, a novel control strategy developed under this project and reported in the FY 2014 annual report was shown to reduce the dc link capacitor (the largest single component) in the ac-dc stage by 60%. Because passive components currently contribute more than 30% to the charger cost, weight, and volume in state-of-the-art Si-based technology, the approach proposed in this project provides enabling technologies to produce low-cost, light, compact, and highly efficient OBCs and converters.

Approach

Our strategy to address the problems of state-of-the-art OBCs and dc-dc converters is multifold.

- Push the envelope on functional integration of the traction drive, 14 V dc-dc converter, and OBC.
- Take up the challenge of introducing WBG materials, specifically GaN, into automotive applications to determine what performance, packaging, cost, and efficiency benefits can be gained.
- Perform analysis, modeling, and simulation that lead to a functional prototype meeting VTO OBC specific power, power density, and efficiency requirements while significantly reducing the current cost levels.
- Design, build, test, and demonstrate prototypes.

- Work with U.S. DRIVE to develop insights and lessons learned from the automotive community pertinent to dc-dc converters and OBCs.
- Collaborate with industry stakeholders, universities, and other national laboratories to maximize the impact of this work.

Three technical approaches, based on converter topology, advanced semiconductor and magnetic materials, and control strategy, are being pursued. First, in power conversion topology, integrated bidirectional WBG OBCs (Figure 1) are being developed that (a) use traction drive inverters and motors as part of the charger converter, (b) provide galvanic isolation, (c) provide an integrated function for dc-dc conversion of HVs to 14 V, and (d) use soft switching at the dc-dc stage to reduce electromagnetic interference and improve efficiency. A key component in the proposed technology is a WBG isolation converter that is used to charge not only the HV traction battery but also the 14 V battery for vehicle accessory loads. It includes a high-frequency transformer, dc filters, and WBG switches (Figure 2).

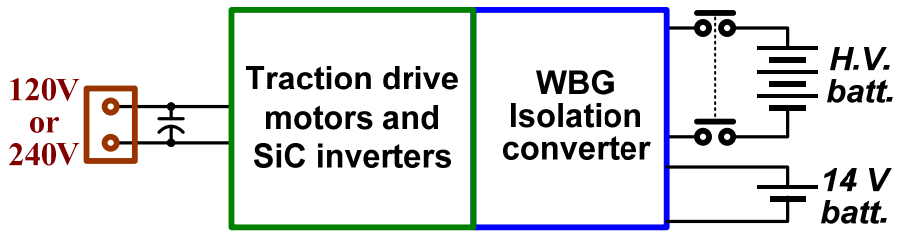


Figure 1: Conceptual diagram of an integrated OBC.

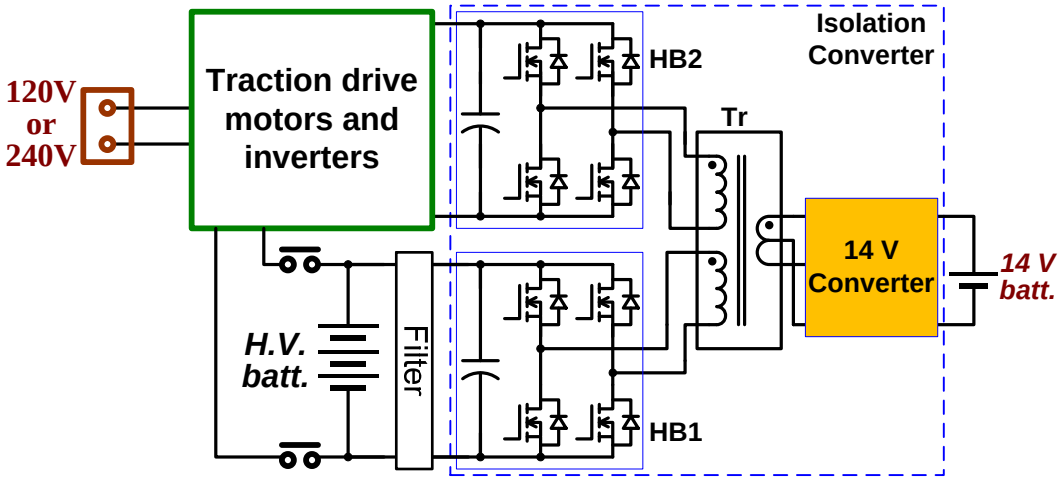


Figure 2: Proposed integrated OBC using a three-port isolation converter.

Second, increasing power density and specific power without compromising efficiency is being aggressively pursued by exploiting high switching frequency with WBG devices (especially GaN switches) and using advanced soft magnetic materials (nanocomposites) to drastically reduce the cost, weight, and volume of the ac and dc filters and isolation transformer. Because the availability of WBG power modules is limited, SiC and GaN devices are purchased or obtained directly from device vendors; they are tested, characterized, and packaged for use in converter design and prototype development. Prototypes will be built and tested, first using SiC devices—for which wafer processing and device fabrication technologies have advanced to a stage such that SiC MOSFETs and other switches are available commercially—and then GaN switches as that technology matures and devices with high current ratings become available.

Finally, a control strategy for the isolation converter has been developed to shrink the bulky dc link capacitor. Without adequate control, this bulky capacitor is necessary to filter out the large voltage ripple—with twice the grid supply frequency—inherent in single-phase ac-dc converters. The proposed control strategy enables a 60% reduction in the ripple current and thereby a significant size reduction in the bulky dc link capacitor in the front ac-dc converter.

Figure 2 shows a proposed integrated OBC that uses the traction drive as the OBC front converter and a three-port isolation converter for charging both the HV propulsion battery and the 14 V accessory battery. The three-port isolation converter uses dual active H-bridge converter with soft switching and synchronous rectification and shares the converter (HB1) and transformer with the 14 V battery charger. The proposed integrated OBC is capable of bidirectional power flow, a desirable function for smart grid applications.

The proposed integrated OBC is flexible and can be applied to most traction drive systems, including (a) single/dual inverter and motor (Figure 3), (b) segmented inverter traction drive (Figure 4), and (c) systems with a boost converter (Figure 5). Moreover, the isolation converter can be applied to stand-alone OBCs (Figure 6).

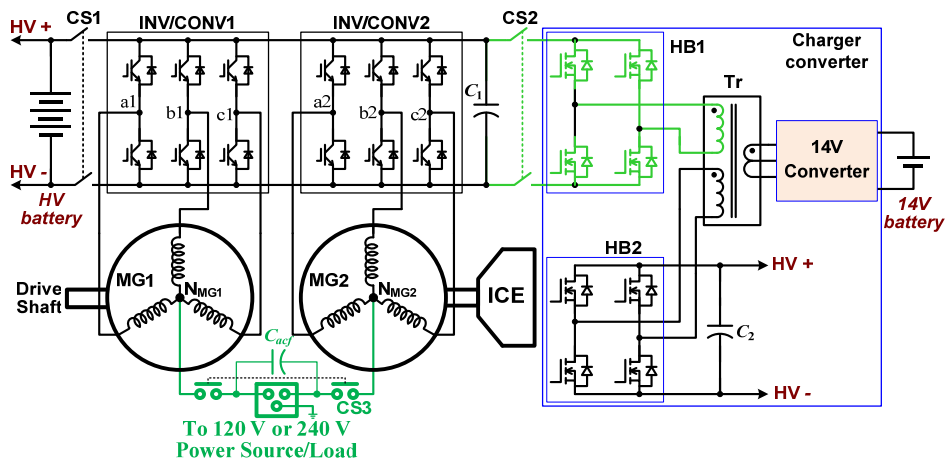


Figure 3: Integrated OBC applied to traction drive system with dual inverter and motor.

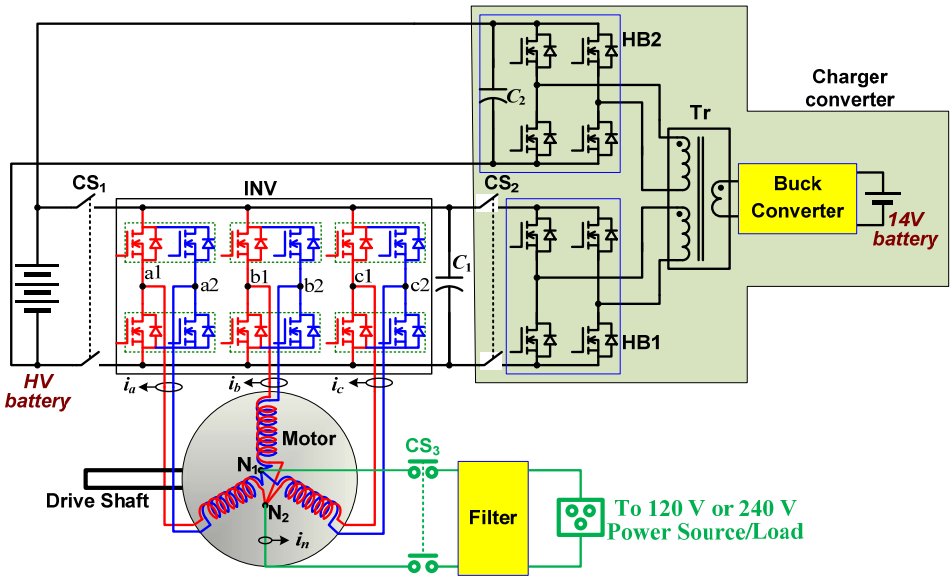


Figure 4: Integrated OBC applied to a segmented traction drive.

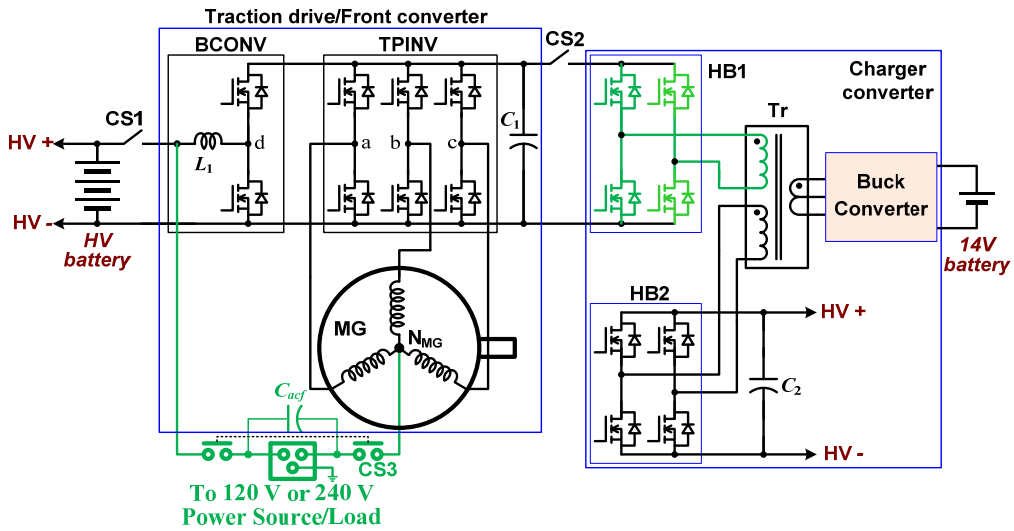


Figure 5: Integrated OBC applied to traction drive system with a boost converter.

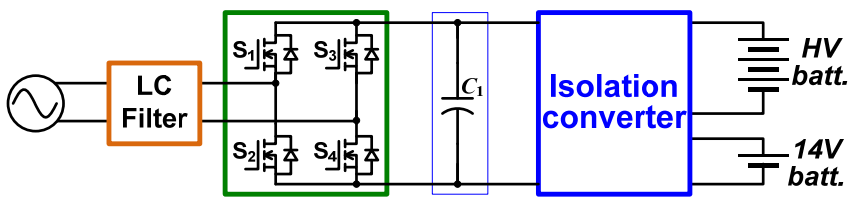


Figure 6: The isolation converter applied to a stand-alone OBC.

Results and Discussion

Work for FY 2016 focused on developing a 6.6 kW GaN-based isolation converter and an integrated OBC using the GaN isolation converter.

Because of the HV rating of 650 V and normally off nature, the latest GaN switches made by GaN Systems were tested and characterized. The following tests were performed and design data were collected for use in designing a 6.6 kW GaN isolation converter: (1) static characterization tests, (2) pulse tests, and (3) H-bridge converter tests.

Figure 7 shows the static characterization test setup. Header pins were used to make connections to the small pads for gate, source, and drain on the switch, and a steel cylinder and springs were used to adjust contact pressures to ensure good electrical conductions. Figure 8 shows the static characterization test results. Test results indicated a relatively low threshold voltage (~1.4 V), which must be considered in designing gate drive circuits for these switches. Results on spread of on-resistance were used to select and match the switches for use in the isolation converter design.

Figure 9 shows the pulse and H-bridge converter test circuits for the GaN Systems devices. Tests were conducted at a dc bus voltage of 400 V and a maximum current of 32 A. Figure 10 shows test results. Fast switching times of less than 10 ns and low switching losses were observed, indicating these devices are well suited for high frequency and efficiency dc-dc converter and OBC applications.

Figure 11 plots GaN H-bridge converter test results for efficiency vs. load power at dc bus voltages of 350 V and 400 V and switching frequencies of 100 kHz and 200 kHz. Measured peak efficiencies are 98.5% at 350 V and 100 kHz, 98.3% at 400 V and 100 kHz, 96.3% at 350 V and 200 kHz, and 96.4% at 400 V and 200 kHz.

Figure 7: Static characterization test setup using pressure contacts.

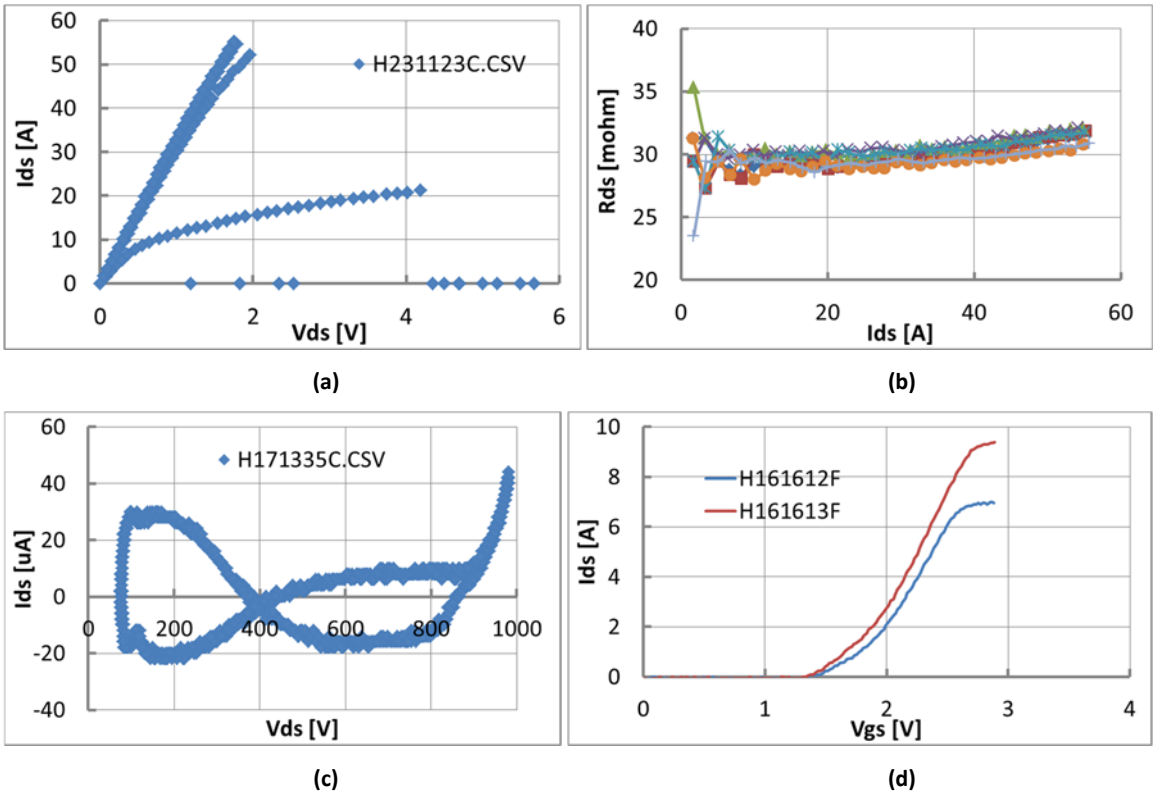


Figure 8: Static characterization test results: (a) I-V curves as the gate source voltage (Vgs) stepped from 0.5 V to 6.5 V in increments of 1 V, (b) spread of on-resistance [Rds(on)] of eight samples at Vgs = 6.5 V, (c) breakdown voltage, and (d) gate threshold voltage.

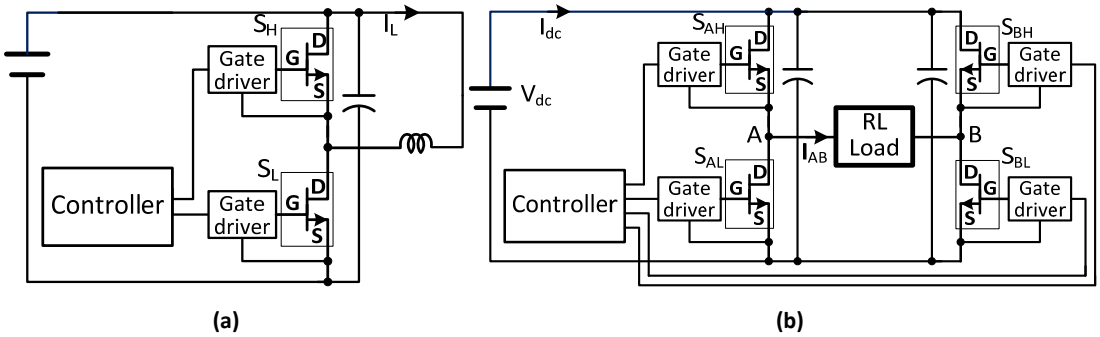
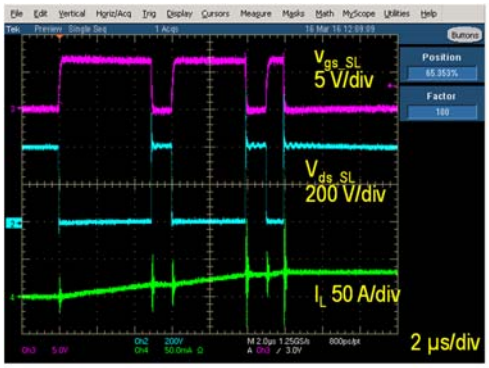
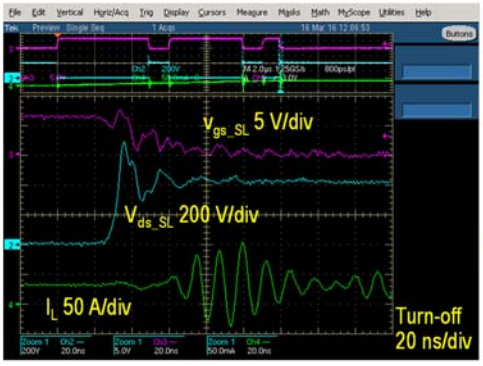
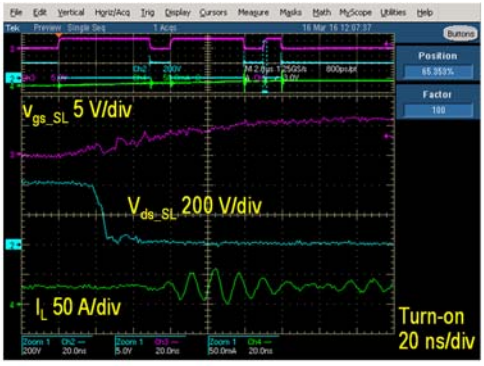


Figure 9: Pulse and H-bridge converter test circuits [(a) and (b), respectively] for the GaN Systems devices.



(a)





(b) (c)

Figure 10: Pulse test results: (a) pulse test waveforms, (b) turn-off, and (c) turn-on.

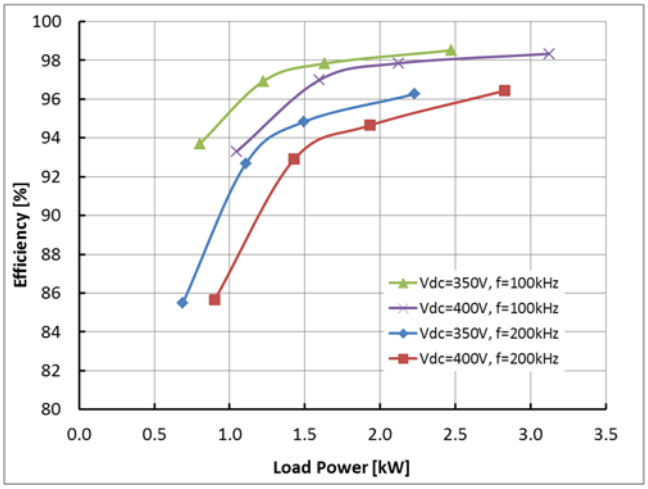
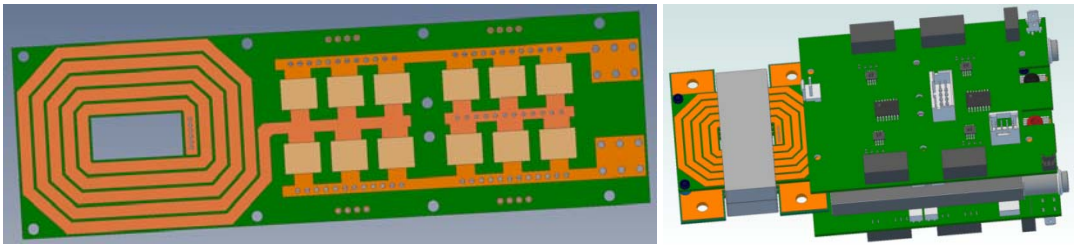


Figure 11: GaN H-bridge converter test results on efficiency vs. load power at different frequencies and dc bus voltages.

Incorporating the test results, a final design for the 6.6 kW GaN isolation converter was completed. The following optimization steps were taken in producing the final design: (1) losses in the ferrite cores and copper winding were analyzed to determine transformer core size and number of turns for minimizing the total transformer losses and (2) PCB trace layout simulations were performed for the primary and secondary transformer to minimize the parasitic inductance for the H-bridge converters. Figure 12 shows 3-D drawings for the final design for the 6.6 kW GaN-based three-port isolation converter. The converter has dimensions of.6.6 in. × 3.2 in. × 1.8 in.



(a) (b)

Figure 12: Final design for the 6.6 kW GaN-based three-port isolation converter: (a) PCB for planar transformer winding and GaN power plane board and (b) complete assembly.

An aluminum pin fin cold plate measuring 3.18 in. × 4.18 in. × 0.375 in. was designed and built for use in the 6.6 kW GaN isolation converter (Figure 13). 3-D printing was used to facilitate the fabrication of this thin (4 mm thick) pin fin cold plate with fine geometries. Finite element thermal analysis results indicate satisfactory cooling performance as shown in Figure 14.

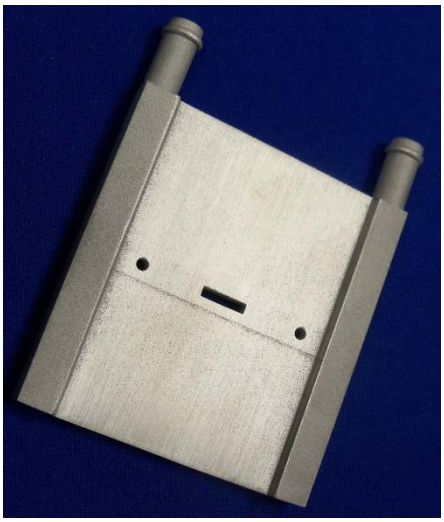


Figure 13: 3-D printed aluminum pin fin cold plate.

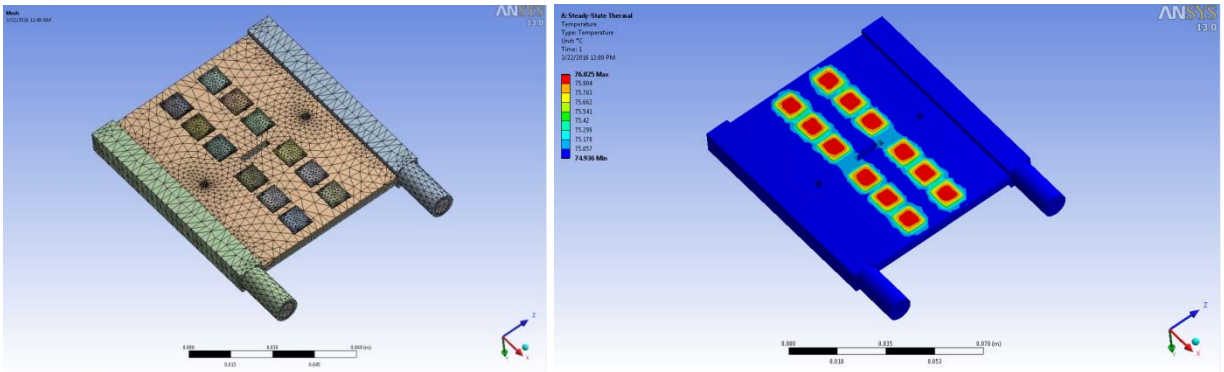
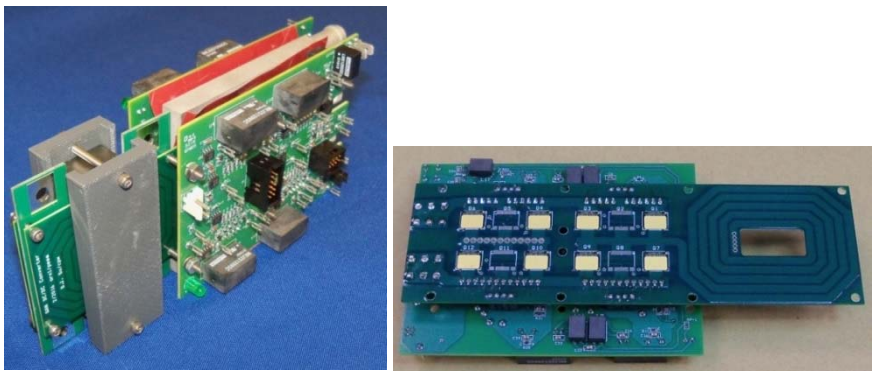


Figure 14: Finite element analysis results for the 3-D-printed cold plate.

A reflow oven at the ORNL packaging laboratory was used to solder the GaN devices to the transformer winding and power plane boards. Measures were taken to ensure the GaN devices were flush at their top sides after soldering so they all will make good contact with the cold plate. The gate drive circuit and PCB layout were designed with emphasis on minimizing gate loop inductance to avoid ringing on the gate source voltage at switching. Working with a magnetic vendor, customized ferrite cores for the planar transformer were designed and fabricated. Figure 15 shows photos of the 6.6 kW GaN isolation converter prototype. A digital signal processor (DSP) control board using the latest Texas Instruments dual-core chip, TMS320F28377D, was used to implement high-speed, high-resolution PWM control loops (Figure 16).

The 6.6 kW GaN isolation converter was tested with a resistive load bank at different switching frequencies. Figures 17–19 show a photo of the test setup, typical operating waveforms at switching frequencies of 100 kHz and 200 kHz, and measured converter efficiency, respectively. Measured peak efficiencies are 99.0% at 100 kHz and 97.5% at 200 kHz.



(a) (b)

Figure 15: Photos of (a) the 6.6 kW GaN isolation converter prototype and (b) the assembled power and gate drive boards.

Figure 16: Digital signal processor board using the latest Texas Instruments dual-core chip.

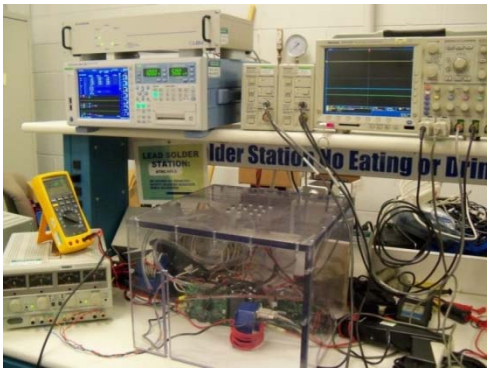
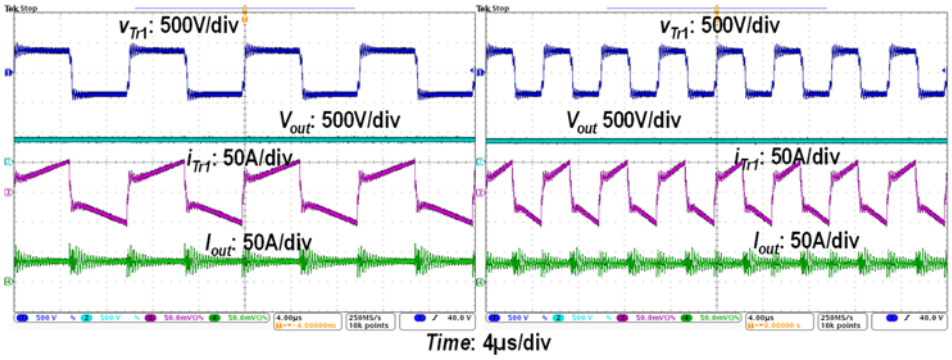


Figure 17: GaN isolation converter test setup.



(a) (b)

Figure 18: GaN isolation converter test results showing operating waveforms (a) at fsw = 100 kHz and (b) at fsw = 200 kHz.

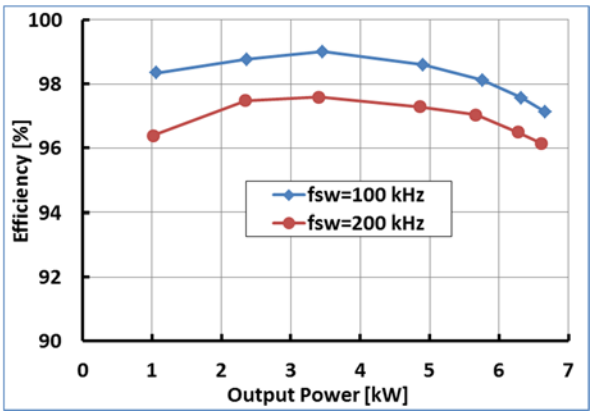


Figure 19: GaN isolation converter test results showing measured GaN converter efficiency.

Table 1 gives a comparison of the GaN-based isolation converter and a 5 kW Si-based counterpart. The GaN-based converter achieved a 50% reduction in volume, 75% reduction in weight, and peak efficiency of 99% vs. 98.4% for the Si-based counterpart at 2.5 times the switching frequency. The GaN converter prototype has a power density of 10.5 kW/L and specific power of 9.6 kW/kg vs. 3.7 kW/L and 1.5 kW/kg for the Si-based converter.

Table 1: Comparison of GaN- and Si-based isolation converters

Text	Si isolation converter	GaN isolation converter	GaN to Si ratio
Volume (L)	1.34	0.63	0.47
Mass (kg)	3.27	0.69	0.21
Peak efficiency (%)	98.4 (40 kHz)	99.0 (100 kHz)	1.0

The 6.6 kW GaN charger converter was then integrated with a 100 kW segmented inverter to test its functionality as an integrated OBC. The segmented inverter was built using six 1,200 V, 120 A dual-pack SiC MOSFET modules and four film dc bus capacitors with a total capacitance of 880 μF, and a 36 cm by 12.7 cm cold plate. 3-D-printed parts were used to make the inverter easily reconfigurable as a dual three-phase inverter or a segmented three-phase inverter. In addition, an induction motor with ratings of 14.92 kW, 230 Vrms, and 45.4 Arms were used as a traction motor in the tests. The motor has two sets of stator windings with all leads accessible and thus is well suited for the segmented inverter.

Figures 20–22 show a photo of the test setup, typical operating waveforms at charging power levels of 3.6 kW and 6.6 kW, and measured OBC system efficiency at a grid voltage of 240 V, respectively. Measured OBC system peak efficiency is 96.6%, a 2.2 % point improvement over the Si-based counterpart.

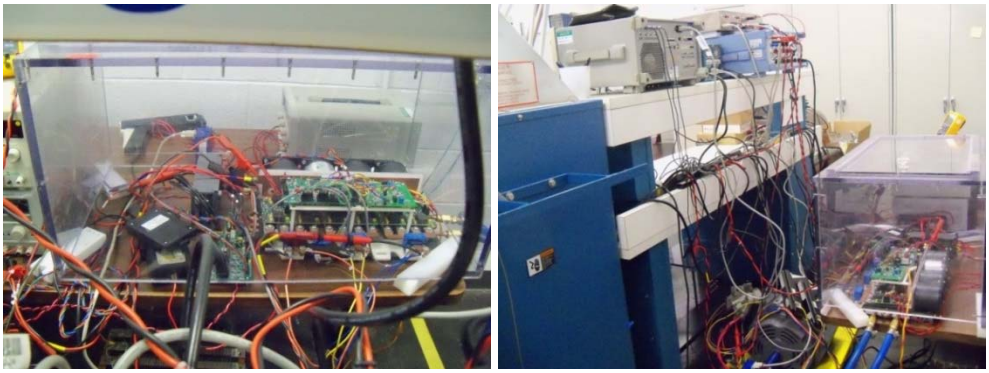
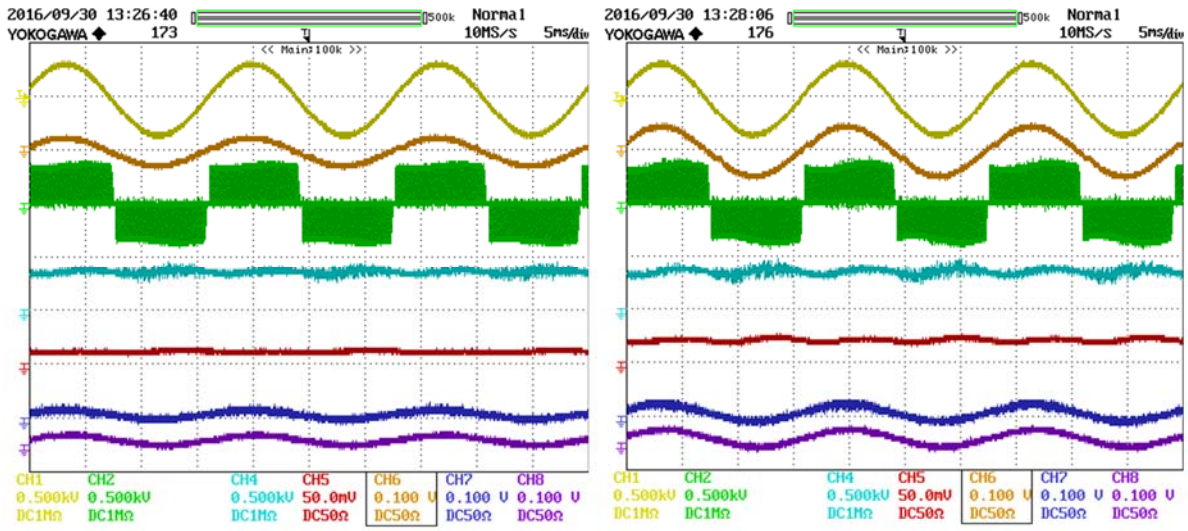


Figure 20: Setup for testing the integrated OBC using the GaN converter and a segmented traction drive.



(a) (b)

Figure 21: Test results–typical operating waveforms for the integrated onboard charger system at charging power levels of (a) 3.6 kW and (b) 6.6 kW.

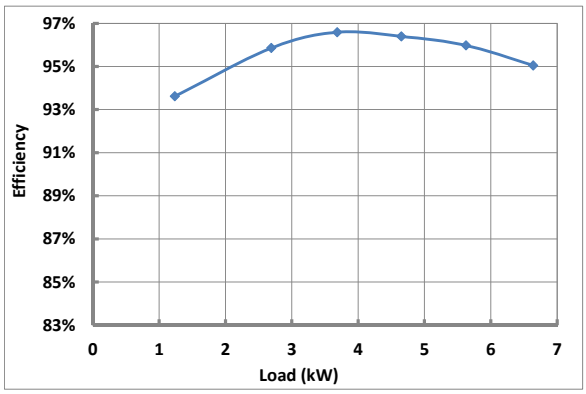
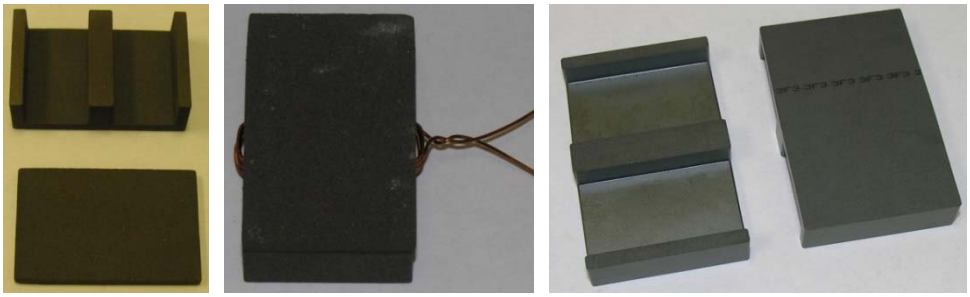


Figure 22: Integrated onboard charger system test results showing measured system efficiency at grid voltage of 240 V.

Working with Aegis Technology, ORNL had generated a transformer core design using Aegis's low-loss nanocomposite magnetic powder material and had printed E-cores at ORNL's manufacturing demonstration facility in FY 2015. In FY 2016, an inductor using the printed cores was fabricated and characterization tests were carried out. Figure 23 shows photos of the printed cores and inductor and similarly sized commercial ferrite cores for comparison.

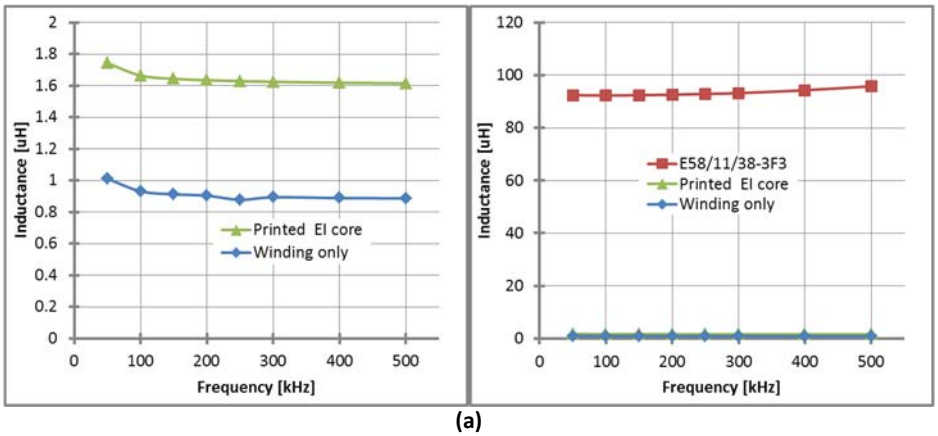


(a) (b) (c)

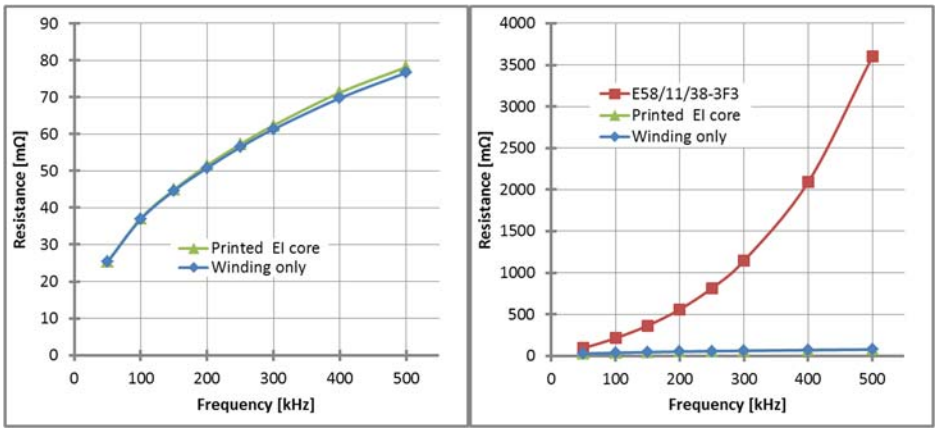
Figure 23: Photos of the ORNL printed cores (a) and inductor (b) and commercial ferrite cores (c) for comparison.

Figure 24 shows measured inductance and resistance for the inductor using the printed cores, an air core (winding only), and an inductor using the commercial ferrite cores (E58/11/38-3F3). Compared to the air core, the inductance values increased less than 2 times with the printed inductor while an increase of about 100 times was measured with the commercial ferrite cores. However, no changes below 300 kHz in resistance with or without the printed cores were observed in comparison to a 4 to 47 times increase with the commercial cores.

The test results indicate there are a significant number of pores or air gaps in the printed cores that substantially reduce the effective permeability of the cores. Future work is needed to improve the printing processes to enhance the density. Another option would be to create 3-D-printed molds with a desired shape and geometry for cores and sinter nanocomposite magnetic powders in the molds.



(a)



(b)

Figure 24: Measured inductance (a) and resistance (b) of the inductor using the printed cores or an air core and an inductor using a commercial ferrite core.

Conclusions and Future Directions

This project is aimed at leapfrogging existing Si-based charger technology to address charger and converter cost, weight, volume, and efficiency by overcoming the limitations of current Si semiconductor and magnetic materials. The multipronged approach involves using WBG devices, including those made with SiC and GaN; advanced magnetic materials; and a novel integrated charger architecture and control strategy.

Under this multiyear project, a new integrated OBC and dc-dc converter architecture has been developed that integrates the segmented traction drive, a 14 V dc-dc converter, and an HV battery charger dc-dc converter. The new topology significantly reduces the number of components: it achieves a 47% reduction in power circuit components alone, not counting savings in the gate driver and control logic circuits, translating to a 50% reduction in cost and volume compared with existing stand-alone OBCs. In addition, WBG-based devices are used in the converter and inverter to further reduce the cost, weight, and volume of the passive components and improve system efficiency. A control strategy for the charger isolation converter was also developed to reduce the battery ripple current inherent in single-phase ac-dc converters. The control strategy was shown to reduce the ripple current by 60%, enabling a corresponding reduction in the bulky dc link capacitor in the active front end converter.

A 6.6 kW GaN charger converter was designed and built using the latest GaN Systems GaN transistors; a 3-D printed cold plate; HV heavy copper PCB power planes; low-voltage (14 V), high-current PCB power planes; and a planar transformer. The converter has a high power density of 10.5 kW/L and specific power of 9.6 kW/kg vs. 3.7 kW/L and 1.5 kW/kg for a Si-based converter. Test results also show higher efficiency for the prototype converter than for Si-based analogues—even at a 2.5 times higher switching frequency.

A 6.6 kW integrated WBG OBC prototype using the GaN-based charger converter and a SiC segmented traction drive was assembled and successfully tested. Test results showed it to have a peak efficiency of 96.6%. The test results also show an improvement of more than 2 percentage points over the Si-based counterpart.

Test results for a 3-D-printed magnetic core using nanocomposite magnetic powders indicate the printing processes need to be improved to enhance the degree of densification. Another option would be to 3-D-print molds with the desired shape and geometry for cores and sinter nanocomposite magnetic powders in the molds.

FY 2016 Presentations/Publications/Patents

1. G. J. Su, “Innovative technologies for converters and chargers,” presented at the DOE Vehicle Technologies Office 2016 Annual Merit Review, June 7, 2016, Washington, DC.
2. G. J. Su and L. Tang, “An integrated onboard charger and accessory power converter for traction drive systems with a boost converter,” presented at the 8th IEEE Energy Conversion Congress and Exposition (ECCE 2016), pp.1–6, September 18–22, 2016, Milwaukee, Wisconsin.
3. G. J. Su, “Innovative technologies for converters and chargers,” presented at the United States Council for Automotive Research LLC, U.S. DRIVE Electrical and Electronics Technical Team meeting, September 29, 2016.

3.3 Gate Driver Optimization for WBG Applications

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Contract No.: DE-AC05-00OR22725

Abstract/Executive Summary

This project addresses a technology gap resulting from the consequences of repeated fast current and voltage transitions in wide bandgap (WBG) –based drive systems and the deleterious effect they can have on system and motor reliability over time. By providing enhanced control and optimization of the gate drive, through dynamic closed-loop slew rate limiting of di/dt (instantaneous current change rate) and dv/dt (instantaneous rate of voltage change over time), fast-switching WBG-based drive systems can achieve higher system reliability, power density, and efficiency, leading to increased market acceptance at a lower system cost point.

This project will further the minimization and integration of the electronics required for traction motor drive systems. A gate drive specifically optimized for silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) will be designed, fabricated, and tested in two phases. The first prototype will be built in a benchtop circuit using commercial off-the-shelf (COTS) components, and its operation will be evaluated. This will be followed by the second phase of the project, focusing on the development of the gate drive in a monolithic integrated circuit, advancing high-frequency WBG design-based size reduction benefits.

Accomplishments

The following tasks were addressed during FY 2016. All reporting and presentation requirements were met.

- Board Level Gate Driver Prototyping using COTS Components
  - A board level gate driver design was completed based on commercially available integrated circuits and components. SPICE (Simulation Program with Integrated Circuit Emphasis) simulations of the primary building blocks were performed using models provided by commercial suppliers. In some cases, SPICE models were not available and suitable representative models were generated.
  - The design was broken into two primary building blocks: the waveform generator and the feedback circuits. Two separate designs were completed for the waveform generator. The initial design was based on steering current sources to generate the complex multistep gate drive waveform and relied on emitter-coupled logic (ECL) circuits for the fast timing requirements of this architecture. A fast timing board was designed and fabricated implementing this approach. A second design allowed significantly reduced timing requirements and used a complex programmable logic device (CPLD) for timing generation coupled with four commercial gate driver integrated circuits, diode summing circuits, and a high-performance signal buffer for the

gate drive. A printed circuit board (PCB) design was completed for each of the building blocks, and the boards were fabricated and loaded with components.
    - The second, less timing intensive method was selected for use in the prototype system, and each of the associated PCBs was tested and functioned as expected.
    - These two custom boards were combined with a clamped inductor test board to form a complete drive system having a variable threshold gate drive waveform.

- Bench Test COTS Gate Driver with WBG Devices
    - The two circuit PCBs of the previous task were combined to drive a SiC power MOSFET. The power device source lead inductance was used as a sensing element and the associated voltage (Ldi/dt) was input to the feedback circuits to provide the gate drive rising edge threshold value (V_{T1}) and the gate drive falling edge threshold value (V_{T2}).
    - The SiC power MOSFET was configured to switch a clamped inductor load, allowing observation of the associated fast switching transients: dv/dt of the device drain to source voltage (V_{DS}) and di/dt of the device drain to source current (I_{DS}).
    - Testing of the combined system was initiated. Initial results show that although the individual system modules function as expected, additional effort is needed to fully realize a working, closed loop, benchtop prototype system.

- Iterate and Finalize Gate Driver Design
    - Although several iterations of the active gate drive (AGD) system modules were completed and tested in FY 2016, closed loop testing of the complete benchtop AGD prototype as a system was completed in only a limited fashion due to a number of technical challenges that occurred throughout FY 2016. These challenges limited the full realization and characterization of a closed loop, benchtop, AGD prototype constructed entirely from COTS components.
    - The experience of building and testing a closed loop, benchtop AGD prototype based on COTS components supports the assertion that a design of this level of performance (fast rise and fall times, precise timing requirements, wide gate drive voltage swings) is much better suited for custom integrated circuit implementation than for COTS implementation.

- Integrated Circuit Fabrication Process Selection
    - Using the design requirements generated during this research in FY 2015 and FY 2016, a set of general requirements was generated for the ideal integrated circuit process targeted for eventual single-chip integration of this design.
    - General specifications for the target process include the availability of a number of device types including NMOS and PMOS transistors with operating voltages ≥ ~20 V, elevated temperature operation (≥175ºC), multiple metallization layers including a "thick" metal for power routing, and available cell libraries with associated SPICE models and process design kits to minimize circuit design time. Both silicon and silicon-on-insulator (SOI) processes were considered.
    - An SOI fabrication process was selected from present commercial offerings for full integration of the AGD circuit (XT06 0.6 micron Modular Trench Isolated SOI Technology Process available through X-Fab). This process includes the basic device types needed [low-, medium-, and high-voltage NMOS and PMOS transistors; three metal layers with a thick third metal layer for power routing; and an extensive library of passive devices, digital circuits, and complex analog functions including operational amplifiers (opamps), comparators, bandgap references, and analog-to-digital and digital-to-analog converters]. In addition, the process uses trench-isolated SOI technology capable of operating at temperatures up to 225ºC, making it ideal for automotive and industrial applications.

Many of the technical challenges encountered in the COTS realization of the proposed advanced gate drive system were addressed during FY 2016, further supporting the assertion that improved gate drives for SiC devices are feasible and should produce the expected benefits. These lessons learned will provide a strong technical foundation for future closed loop AGD realization and validation.

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Introduction

WBG devices, primarily SiC and gallium nitride, have characteristics that can lead to dramatic benefits in a variety of power electronics applications. These include higher temperature and higher frequency operation, smaller device and overall system sizing, and greater operational efficiency. Their ability to switch at higher frequencies than their silicon counterparts can also lead to significant volume reduction in associated passive components, yielding second-order benefits in reduced material costs and weights. For every 10% reduction in the weight of a vehicle, a 6%–7% increase in fuel economy can be realized. For this reason, significant attention has been given to the miniaturization and lightweighting of all components and systems in a vehicle by automotive original equipment manufacturers. The rapidly escalating move from the use of power silicon to WBG devices to capture some of these advantages entails revisiting and optimizing their interplay with ancillary circuits and systems to truly exploit their unique characteristics.

Available commercial gate drives are not optimized for use with WBG devices. They have historically been developed for silicon devices and cannot exploit the distinctions that WBG semiconductors can offer traction drive systems. The faster di/dt and dv/dt switching capabilities of WBG devices can impose implications that need to be addressed at a system level. Fast switching can reduce the reliability of motor insulation by creating pinholes in the insulation that eventually can cause arcing and failure of the motor. To combat this possibility, additional costs must be incurred for higher rated winding insulation, imposing increased motor and cabling costs and resulting in larger and heavier motors. Additionally, fast switching transients can induce unwanted circulating currents, resulting in pitted bearings. Fast voltage and current transitions can also necessitate added electromagnetic interference (EMI) filtering requirements to protect sensitive electronic systems from electronic interference, adding further costs and increased system volume and weight.

This project addresses the cost and volume barriers to achieving the DOE traction drive system goals of $8/kW and >4 kW/L power density. To achieve these goals, a cost-effective, efficient topology for monitoring and controlling the dynamic slew rate of a WBG gate drive will be developed to drive a SiC MOSFET motor leg. The design will ultimately be implemented in an integrated circuit to minimize the volume and reduce packaging issues.

This work can serve as an enabling technology, which, if implemented in a high-temperature process, can be used for future integrated motor/inverter systems.

The design will result in

- higher inverter reliability and efficiency through monitoring and using dynamic slew control,
- 50% reduction in gate drive electronics volume by drive integration,
- higher temperature capability (>200°C) through use of SOI technology,
- higher motor reliability,
- reduced insulation breakdown,
- reduced bearing currents,
- lower cost gate drive systems through parts reduction,
- gate driver integration, and
- decreased EMI filtering.

This project will advance the technology of gate drives and hasten the deployment of WBG devices in vehicular traction drives by significantly increasing power density and lowering cost, circuit volume, and weight while increasing reliability and allowing the opportunity to move toward an integrated, high-temperature-capable traction drive system.

Approach

An active gate driver topology was developed to address the technology gaps associated with WBG-specific gate drives. This architecture was simulated using a custom-designed circuit topology with a vendor-supplied WBG device model in PSpice (a commercial SPICE derivative) and prototyped using COTS components. The four tasks identified for carrying out the project goals in FY 2016 are as follows.

- Task 1. Board Level Gate Driver Prototyping using COTS Components
  - Design and implement a benchtop prototype AGD system based entirely on commercially available components (COTS components).
- Task 2. Bench Test COTS Gate Driver with WBG Devices
  - Test the fabricated advanced gate driver prototype system using a SiC power MOSFET load.
- Task 3. Iterate and Finalize Gate Driver Design
  - Optimize the AGD benchtop prototype through improved prototype design and construction to maximize performance.
  - Produce a final AGD benchtop system architecture.
- Task 4. Integrated Circuit Fabrication Process Selection
  - Investigate commercially available integrated circuit processes for implementation of an AGD system chip.

The project strategy was to incorporate lessons learned from previous gate drive research at ORNL and the University of Tennessee, as well as synergies with previous projects focused on SiC gate drivers; to incorporate di/dt and dv/dt control through di/dt sensing; to generate a variable threshold gate drive waveform with feedback electronics; and ultimately to develop a high-temperature-capable gate driver integrated circuit suitable for integration with a traction motor to realize size, volume, and DOE cost targets.

Results and Discussion

Beginning with the advanced gate driver architecture developed and simulated in FY 2015, the AGD topology was modified to incorporate a variable threshold gate drive waveform instead of the variable slew waveform type used in FY 2015 circuit simulations. SPICE simulation results indicated that this new gate drive waveform provided improved control of the di/dt and dv/dt of SiC power switching devices, as compared to more conventional methods based on shaping or slew rate limiting.

The modified AGD general topology is shown in Figure 1(a) and the variable threshold gate drive waveform produced in Figure 1(b). A timing generator circuit provides synchronized timing control for generation of the variable threshold waveform. Feedback circuits capture the di/dt peak voltage generated during both the rising and falling edges of the gate drive waveform, filter these voltages, and then apply appropriate gain and offset to produce the two variable thresholds V_{T1} and V_{T2} [Figure 1(b)] used by the waveform generator.

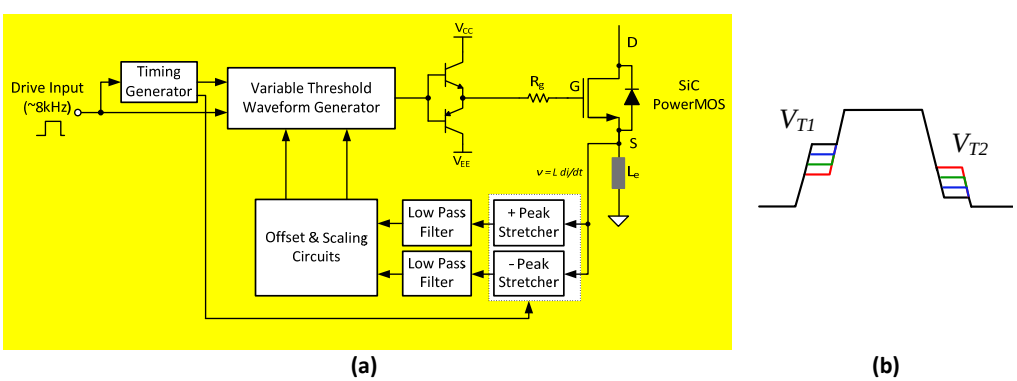


Figure 1: AGD circuit topology selected for COTS implementation incorporating WBG source inductive current sensing for di/dt feedback control (a) and the associated variable threshold gate drive waveform produced (b).

Two different designs of the waveform generator were explored for this research. The initial design used switched current sources to charge a capacitor with the desired waveform followed by two buffering stages to produce the desired gate drive waveform. This design was extensively simulated in PSpice using vendor provided models for all components except for the timing generator function. Realizing a COTS-based design proved to be very challenging due to the unique requirements of this circuit module: 20 V signal swing, high slew rate (~1,300 V/ms), relatively high bandwidth (23.3 MHz), and high output current (1.5 A peak). Only two commercially available opamps were found to meet all of these specifications. The current mode ADA4870 opamp (Analog Devices, Inc.) was selected and incorporated in the design. To provide additional high-current buffering, a bipolar transistor-based diamond driver was placed at the output for driving the SiC power MOS load. Figure 2 shows the initial waveform generator block diagram and a PSpice simulation result performed using commercially available circuits for all components except for the timing generator.

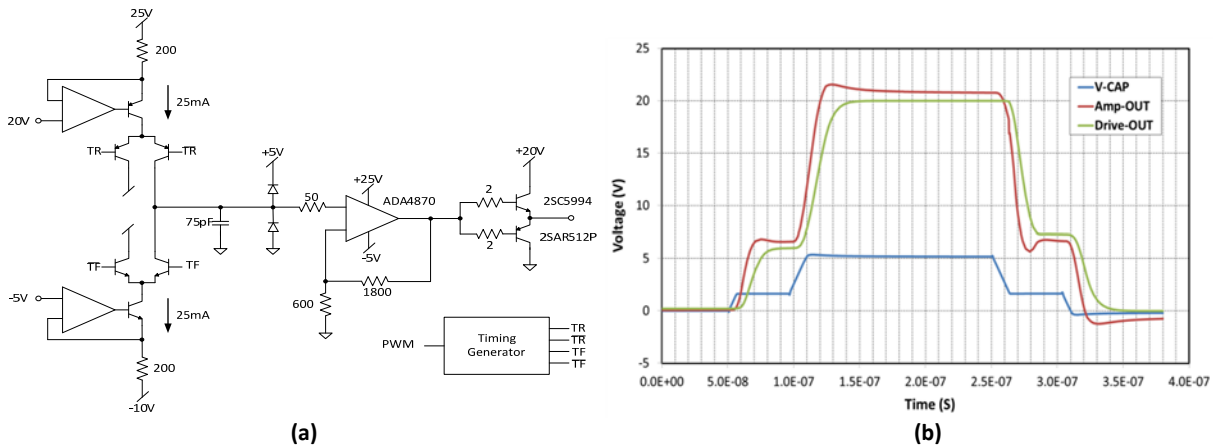


Figure 2: Version 1 waveform generator block diagram (a) and PSpice simulation output waveform (b).

Timing generator circuits were also required for this waveform generator design to control the current sources used to generate the shaped drive waveform. A careful investigation into the requirements for these circuits indicated that using field programmable gate arrays or CPLDs was not acceptable, primarily due to the 1–2 ns delays associated with getting the signals in and out of these reprogrammable digital circuits. These stringent timing constraints are associated with the need for precise control of the current sources for producing signals with very short rise times (5–10 ns). Figure 3 shows an example simulation with these timing requirements produced using PSpice (a commercial SPICE derivative) with circuits modeled using an integrated circuit fabrication process. To meet these demanding timing requirements for the COTS design, a timing generator block was designed and fabricated based on ECL. The fabricated module is shown in Figure 4.

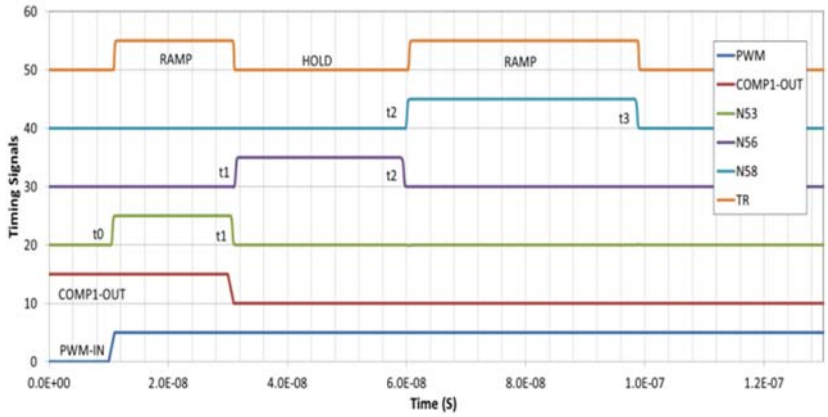


Figure 3: Timing generator PSpice simulation using circuit models from a modern integrated circuit process.

Figure 4: ECL-based timing generator PCB for the initial waveform generator design.

To reduce the waveform generator dependency on highly precise and difficult to produce timing controls, an alternative design was generated that significantly relaxed the timing requirements. In this design, COTS gate drivers were used with a diode network to generate the desired waveforms [Figure 5(a)]. Within the operating supplies of the commercial gate drivers, the supplies can be varied to produce the four desired output voltages: ground, rising threshold voltage (V_{T1}), maximum output amplitude, and falling threshold voltage (V_{T2}). The precise width of the two threshold voltage regions is not critical in this design as the AGD loop will adjust to accommodate variability in these widths. The general topology of WaveGen2 is shown in Figure 5(b). A CPLD generates timing control signals that are galvanically isolated from the gate driver using commercial isolators. This provides both electrical isolation and signal level shifting. Commercial gate drivers are used to provide a high-current drive capability for charging a hold capacitor through the diode network. Care was taken to properly select diodes to minimize the forward voltage drop and minimize the parasitic capacitance to minimize charge injection. The opamp buffer and diamond driver used in the initial waveform generator design were used here as well to buffer the gate drive signal.

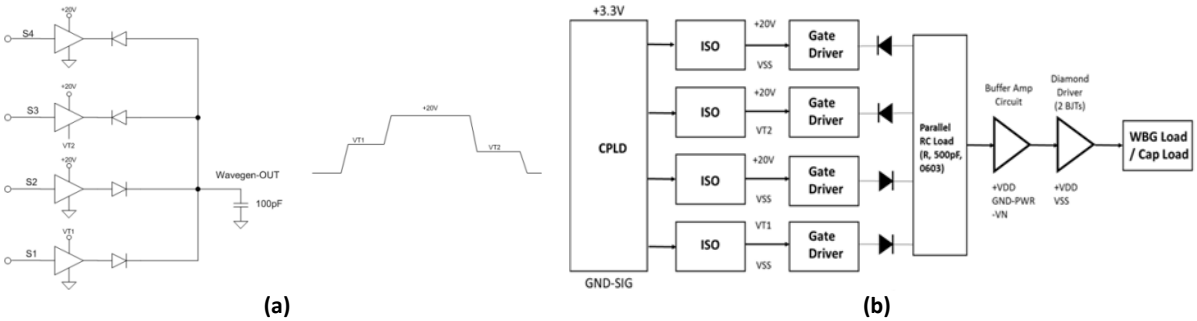


Figure 5: Alternative waveform generator (WaveGen2) simplified functional diagram (a) and overall circuit block diagram (b).

The fabricated WaveGen2 circuit is shown in Figure 6. The board was populated with a load capacitance of 2nF to simulate a large SiC power MOS gate load. Testing this unit produced a very fast gate drive waveform with the ability to separately adjust the rising plateau voltage (V_{T1}) and the falling plateau voltage (V_{T2}). Plots showing measured output waveforms while driving a 2nF load are provided in Figure 7. Some signal overshoot at the edges was observed, which can be minimized through additional circuit optimization. However, the design worked very well and produced very fast rise and fall times (on the order of 15–20 ns total), as demonstrated in Figure 7(b). Theoretically, significant variations in the signal overshoot and threshold plateau width will be readily tolerated by the overall AGD topology, as the control loop will modulate the threshold voltage values to drive the di/dt toward the set point value.

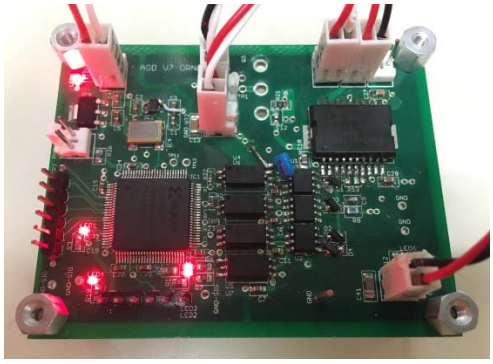
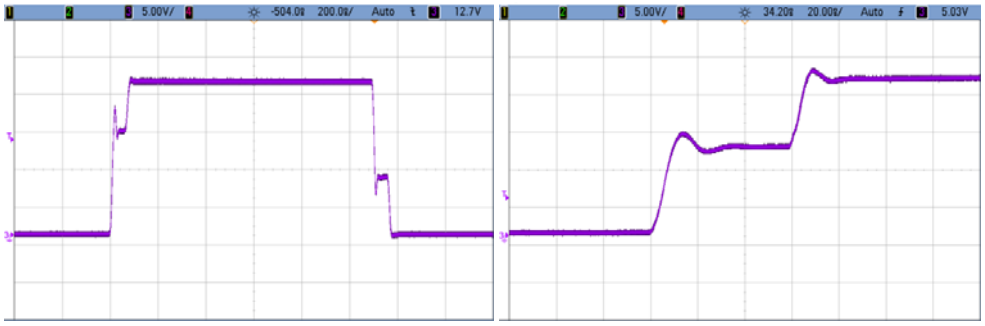


Figure 6: Fabricated WaveGen2 waveform generator module.



(a) (b)

Figure 7: WaveGen2 Measured Waveforms: Rising and falling edges showing the two variable threshold values (a) and a zoom view of a rising edge showing ~7ns and ~5ns rise times in the two transition regions (b).

A feedback circuit board was also designed and fabricated to generate the two threshold values (V_{T1} and V_{T2}) for the waveform generator from the sensed di/dt signal (Figure 8). This board incorporates two similar channels that can be configured to accommodate the specifics of the rising and falling edge di/dt values. Each channel has a peak hold circuit with reset that holds the peak di/dt signal associated with the appropriate drive transition. The held signal is low-pass filtered, and gain, offset, and inversion are applied to produce the threshold voltage signals for the waveform generator module. Test results for this module indicated proper operation with input signals representative of the expected sensed signal. Each channel was configured to provide the appropriate polarity of operation—increasing di/dt produces an increase in V_{T1} and a decrease in V_{T2} for the rising and falling gate drive waveforms, respectively.

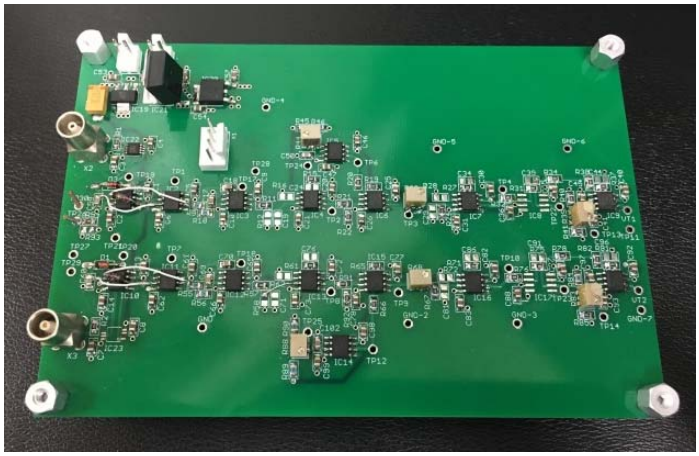
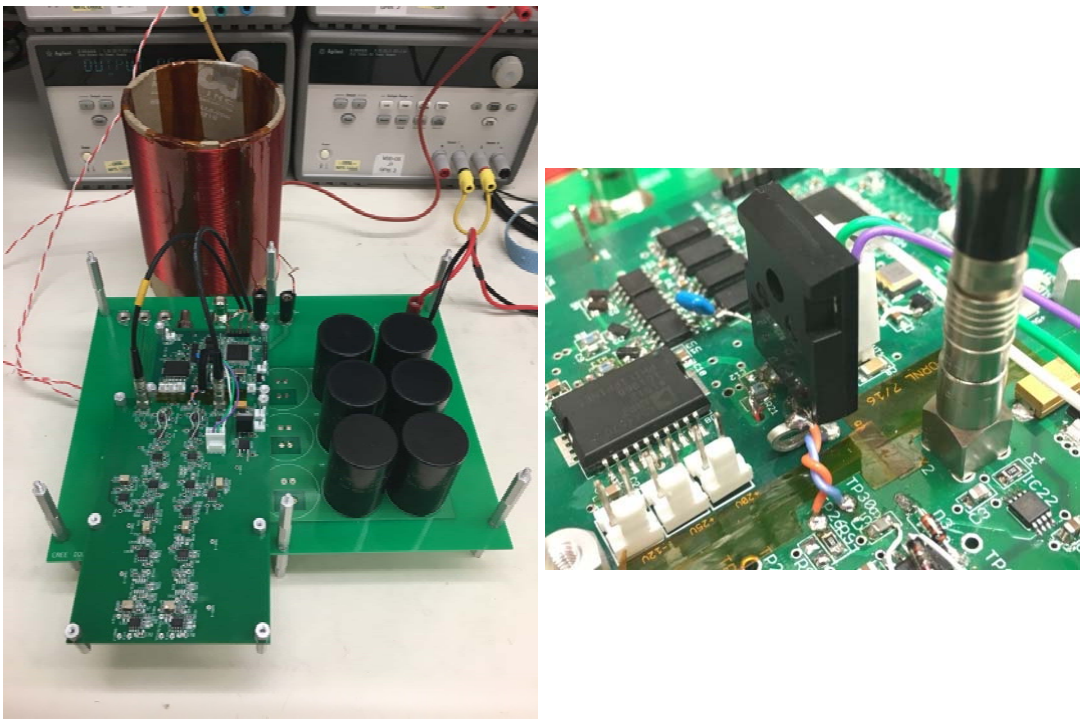


Figure 8: AGD Feedback PCB used in AGD benchtop system testing.

The AGD benchtop prototype unit was assembled by integrating the system modules: the WaveGen 2 PCB, the feedback PCB, and a clamped inductor test board (Figure 9). The clamped inductor test board design (Cree, Inc.) enabled measurement of the power MOS device drain current and drain-to-source voltage. The SiC power MOS switch was mounted on the waveform generator PCB in close proximity to the diamond driver to minimize stray inductance. A small loop was added to the source leg of the SiC switch as a source inductance for monitoring di/dt [Figure 9(b)], and a small pair of twisted wires were used to input the di/dt feedback signal to the feedback PCB. The outputs of the feedback board (V_{T1} and V_{T2}) were input to the waveform generator PCB threshold inputs. Timing signals for resetting the feedback board peak stretcher circuits were provided by the waveform generator PCB CPLD and were connected using short coaxial cables. The leads of the SiC power MOS device were passed through the waveform generator PCB directly into the socket on the clamped inductor test module. The CPLD was designed to be operated from an external pulser and generated the timing signals to enable straightforward control of the gate drive waveform pulse width (duty cycle) and repetition rate (frequency) for testing flexibility. External power supplies were used to power these units, and each board was configured with local voltage regulators and filtering to minimize noise injection.



(a) **(b)**

Figure 9: Benchtop prototype AGD composed of the WaveGen2, feedback, and clamped inductor modules (a) and close-up view of SiC Power MOS device with added source lead inductance (b).

Initial testing of the integrated system indicated that further system integration work was needed for full evaluation of this design. Optimization of each individual unit was performed during testing and construction, but further optimization as an integrated system is needed to fully assess the AGD performance.

In addition to the AGD design and prototyping activities, candidate integrated circuit processes were investigated in preparation for eventual single chip integration of the AGD design. General specifications for the target process were identified; among them are available device types, including NMOS and PMOS transistors with operating voltages ≥ ~20 V; elevated temperature operation (≥175ºC); multiple metallization layers for interconnects, including a "thick" metal for power routing; and analog and digital cell libraries with associated chip layouts, test results, and SPICE models. Both silicon and SOI processes were investigated.

An SOI fabrication process was selected as the best of the current commercial offerings for full integration of the AGD circuit (XT06 0.6 micron Modular Trench Isolated SOI CMOS Technology Process available through X-Fab). This process provides the basic device types needed (low-, medium-, and high-voltage NMOS and PMOS transistors); three metal layers with a thick third metal layer for power routing; and an extensive

library of passive devices, digital circuits, and complex analog functions including opamps, comparators, bandgap references, and analog-to-digital and digital-to-analog converters. In addition, the process uses trench-isolated SOI technology capable of operating at temperatures up to 225ºC, making it ideal for automotive and industrial applications. This process is an excellent candidate for AGD integration as it meets all of the device needs for the AGD.

Conclusions and Future Directions

This project is focused on achieving DOE volume, weight, and cost targets for advanced traction drive inverters while providing a high-temperature gate drive solution enabling an integrated motor-inverter system. It includes development of a circuit to actively monitor and optimally respond to the fast switching characteristics of SiC switches to ensure system reliability, enabling safe use of SiC MOSFETs in drive inverter modules to increase inverter efficiency and reduce system volume and cost.

The research activities of FY 2016 have culminated in the realization of a benchtop prototype of the advanced gate drive system. The system uses an advanced gate drive waveform variable threshold gate drive, which putatively provides improved control of undesired WBG device switching transients, as compared to RC– and slew rate–based conventional approaches to gate drive control. Building on the architecture developed and simulated in FY 2015, efforts were directed toward implementation of the AGD architecture using COTS components for system demonstration and testing. The most difficult module of this system was determined to be the waveform generator. Two waveform generator designs were investigated, the first requiring very fast timing circuits and the final architecture having much relaxed timing requirements. The second design was successfully implemented and functioned well with a 2nF capacitive load. A fast timing generator PCB was also designed and built based on ECL circuits but was abandoned as the alternative design became the apparent technology of choice. In addition, a feedback board was designed to process the di/dt-based waveform and produce the variable threshold values used by the waveform generator to produce the rise and fall plateau voltages. This board was tested on the bench, and modifications were made to optimize its performance. Finally, the three modules (WaveGen 2, feedback, and clamped inductor) were integrated for operation as a complete AGD. Bench testing as a system was initiated using a SiC power MOS device. More testing will be needed before translation of the design to a single integrated circuit.

In many instances, the circuits involved in this design are much better suited to chip integration than to implementation using COTS components due to the much reduced parasitic capacitance and inductance associated with monolithic construction. In addition, as previously detailed, there are commercially available modern integrated circuit processes incorporating the device types needed capable of meeting all specifications of the AGD design.

With the maturation of WBG devices and their continued penetration of the automotive sector, it is expected that a more system level approach to their implementation will be needed in the near future. Optimization of the gate drive for performance, reliability, and cost will be paramount in these efforts. This research will position the ORNL team to initiate SOI integrated circuit implementation of the AGD, an enabling technology for realizing reliable and highly compact WBG-based traction drive systems.

FY 2016 Presentations/Publications/Patents

1. N. Ericson, C. Britton, L. Marlino, S. Frank, D. Ezell, L. Tolbert, and J. Wang, “Gate driver optimization for WBG applications,” presented at the DOE Vehicle Technologies Office 2016 Annual Merit Review, June 8, 2016, Washington, DC.
2. N. Ericson, C. Britton, L. Marlino, S. Frank, D. Ezell, L. Tolbert, J. Wang, and B. Blalock, “Gate driver optimization for WBG applications,” presented at the United States Council for Automotive Research, LLC, U.S. DRIVE Electrical and Electronics Technical Team Project Update Meeting, July 21, 2016.

4.1 Benchmarking Electric Vehicles and Hybrid Electric Vehicles

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Contractor: UT-Battelle, LLC, managing and operating contractor for ORNL
Contract No.: DE-AC05-00OR22725

Abstract/Executive Summary

This benchmarking project provides vital information about the status and developmental trends of electric vehicle/hybrid electric vehicle (EV/HEV) components to DOE VTO for strategic planning of state-of-the-art technologies projects. ORNL's detailed benchmarking reports have received tremendous positive feedback from researchers in academia and industry, as well as other individuals with an interest in EV/HEV technologies. This information serves as a valuable educational resource on EV/HEV architectures, yields a track of lessons learned, prevents reinventing/duplication of advancements, and promotes leap-frog/competitive development. FY 2016 efforts include design assessments and comprehensive dynamometer testing of the electric machine and drive inverter from the 2016 BMW i3 electric vehicle.

Accomplishments

- Designed, fabricated, and assembled the hardware necessary to adapt the 2016 BMW i3 transmission to the dynamometer test cell.
- Successfully integrated ORNL controls with the 2016 BMW i3 motor inverter.
- Conducted comprehensive dynamometer testing of the 2016 BMW inverter and motor to obtain efficiency maps, peak torque, peak power, and many other performance metrics.
- Confirmed published peak torque and power specifications for the 2016 BMW i3 inverter and motor.

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Introduction

The 2016 BMW i3 is an electric vehicle that includes a motor with a published power rating of 125 kW and a torque rating of 250 Nm. The 2016 i3 is sold in the battery-only option with a published range of 80 miles, and the range extender (with small combustion engine) option, with a published range of 160 miles. This first generation vehicle includes a 360 Vdc, 22 kWh lithium-ion battery. The second generation, beginning in model year 2017, includes the option for a 33 kWh battery with a 114-mile battery-only range, and the range extender option with a 180-mile range. This report reviews results from the disassembly of the motor and inverter unit and discusses detailed findings from teardown analyses. Comprehensive dynamometer testing was conducted, and the performance, efficiency, and other operational results are summarized herein.

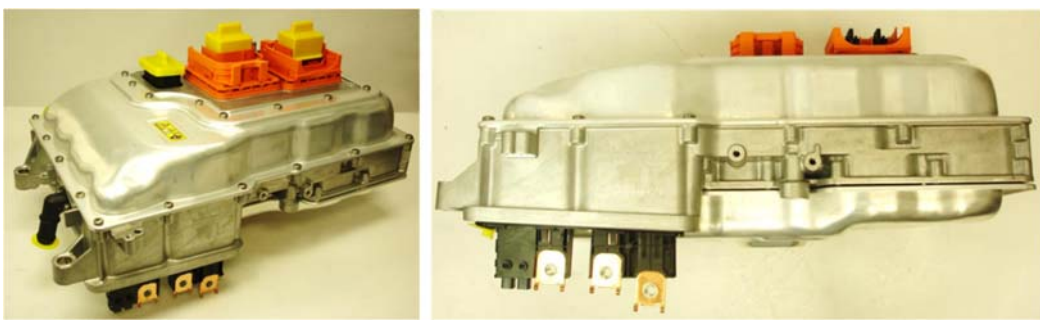
Approach

Automotive manufacturers do not typically publish details about the design, functionality, and operation of EV/HEV technologies, and even published details and specifications must be verified and clarified. For example, single-value power ratings for motors and inverters are often published, but they do not include information about the power capability throughout the operation range (e.g., versus speed), the duration for which this power can be maintained, the efficiency throughout the operation region, and many other important characteristics. Therefore, ORNL performs teardown assessments to obtain comprehensive information on design, functionality, and subcomponent characteristics. Furthermore, components are completely instrumented and tested in a dynamometer test cell to determine operational characteristics such as performance and efficiency. These activities provide the information needed for DOE to warrant a robust program and provide DOE partners and other researchers with valuable information on state-of-the-art EV/HEV technologies.

Results and Discussion

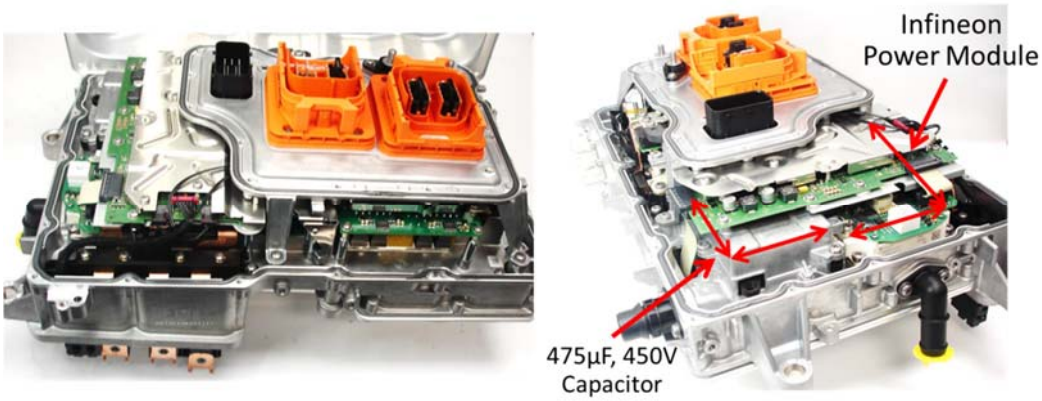
2016 BMW i3 Inverter Design and Functionality Assessments

The BMW i3 inverter assembly shown in Figure 1 contains the motor inverter, dc/dc converter (~360 V to 12 V), and a 3.7 kW battery charger. The mass of the inverter as received was 19 kg. Visible electrical connectors in this figure include two large dc voltage connectors and a small connector for low voltage power supply, communication, and other low voltage signals. After the top cover is removed as shown in Figure 2, key components of the assembly are visible. Circuitry for the 3.3 kW charger is located in the top compartment along with all components of the main inverter, including the power module, a driver board, control board, dc link capacitor, three current transducers, and ac bars.



(a) (b)

Figure 1: 2016 BMW i3 inverter assembly: (a) isometric view and (b) side view.



(a) (b)

Figure 2: 2016 BMW i3 inverter assembly with top cover removed: (a) front and (b) side.

After the control board, interface connectors, and other components are removed, the driver board, power module, and dc link are visible, as shown on the left in Figure 3. The right portion in the assembly shown in Figure 3 contains the passive components and electronics of the 3.3 kW charger. A 475 µF, 450 V capacitor is shown in the top left of Figure 3. The size of this capacitor is much smaller than other systems with comparable power ratings. This is being investigated further. It may be possible that a capacitor is installed on the dc link in the other 3.3 kW charger or perhaps (but not likely) at another location on the vehicle. A detailed examination of the control board components was conducted, and the key items are indicated in Figure 4. Two TriCore Infineon DSPs are noticed, as well as an Altera MAX II EPM570 CPLD chip. Additionally, an AD2S1210 resolver-to-digital (R2D) converter chip was identified. This is the first benchmarked system that does not use a Tamagawa R2D product.

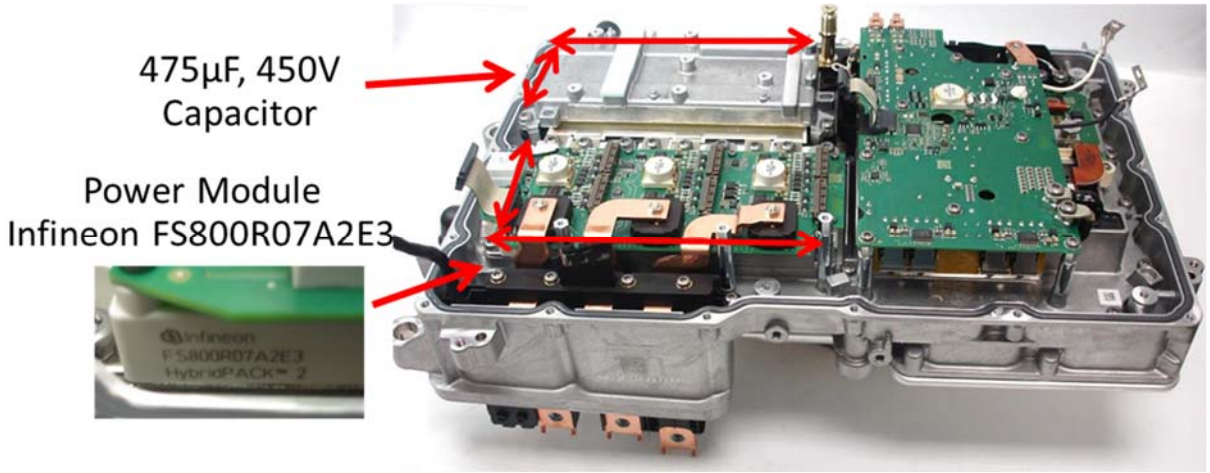


Figure 3: Location of inverter components in 2016 BMW i3 inverter assembly.

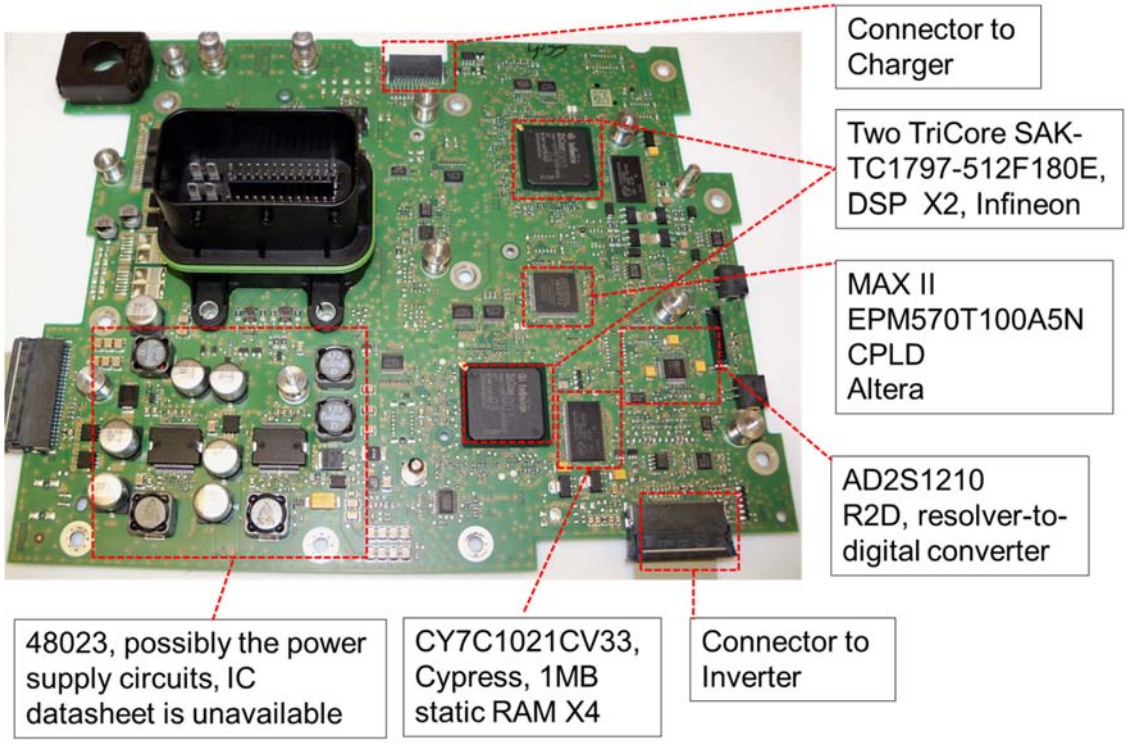


Figure 4: Key components on control board in 2016 BMW i3 inverter assembly.

Detailed component analysis of the driver board for the Infineon FS800R07A2E3 power module was conducted, and key components are shown in Figure 5. The module has a rating of 650 Vdc and 800 A/1600 A peak. It appears that a transformer is included for power isolation on each phase, and three 700 A LEM

HC5F700 current sensors are located on the driver board. Six 2.2 Ω resistors are used for gate drive resistance at the 851 and 951 totem pole output.

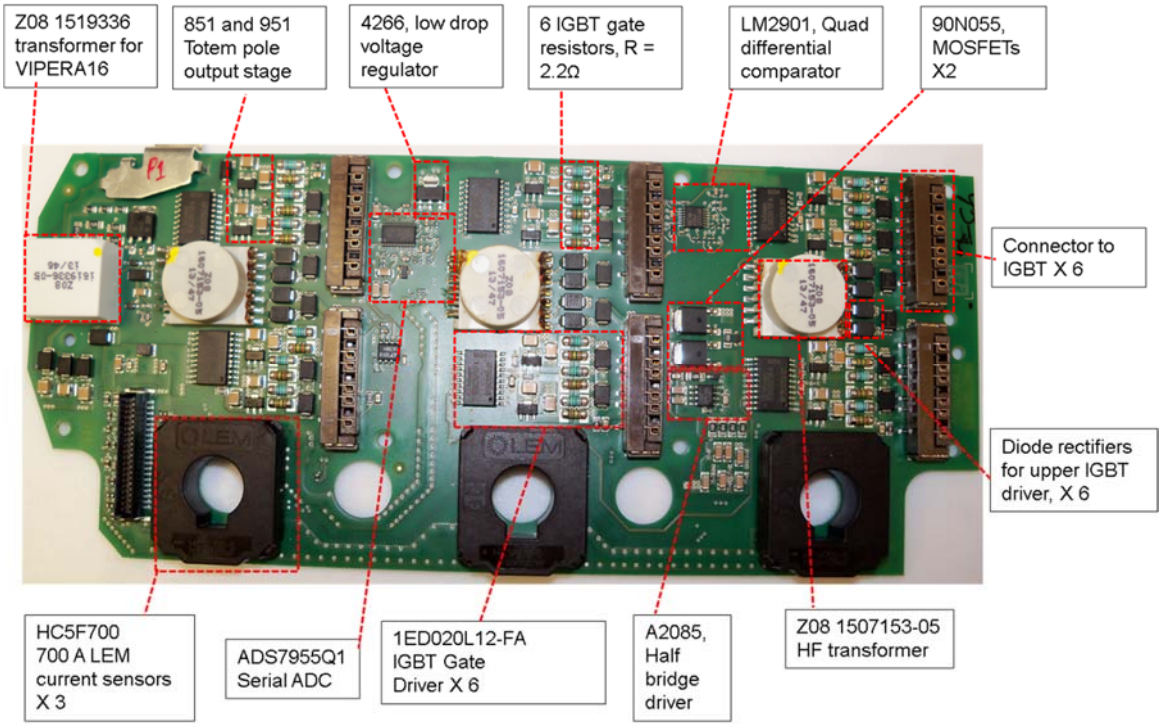


Figure 5: Key components on driver board in 2016 BMW i3 inverter power module.

After removing the gate driver board and plastic power module cover plate, the power electronics devices are visible in Figure 6. It is seen that four insulated-gate bipolar transistors (IGBTs) and four diodes are arranged in a parallel configuration for each switch. As with other Infineon modules, only one gate drive pin and trace is used to drive all four IGBTs in parallel. All connections from the devices to the dc link and ac output are accomplished with wire bonds. The dc bus bars from the capacitor attach to two terminals for each phase, as seen in the lower portion of Figure 6, and ac output terminals are visible in the top portion of Figure 6.

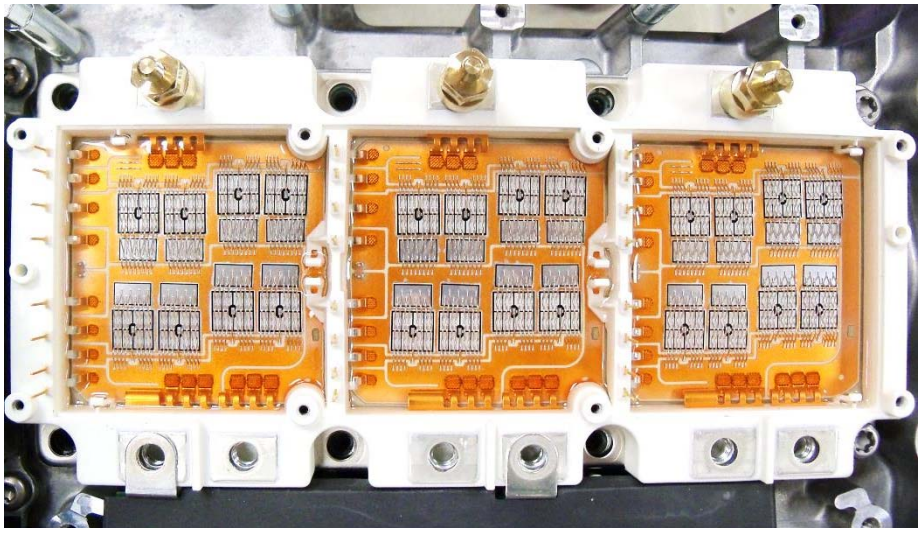


Figure 6: 2016 BMW i3 Infineon three-phase inverter power module with cover removed.

A close-up image of two IGBTs and two diodes is shown in Figure 7. Each IGBT has a cross section of 9.6 mm by 10.3 mm, and each diode has a cross section of 5.4 mm by 9.15 mm.

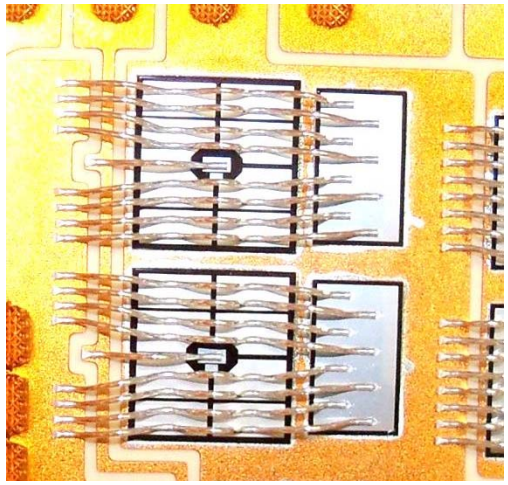
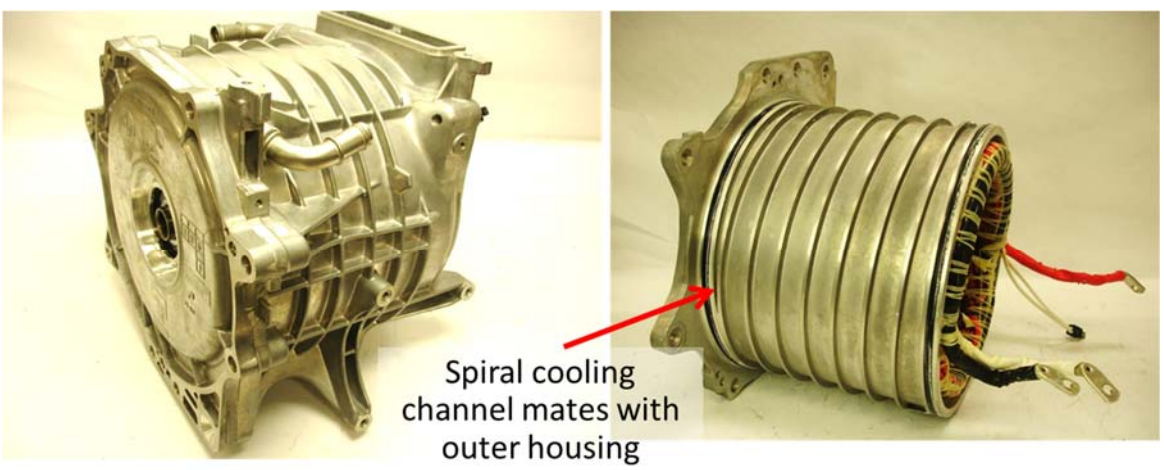


Figure 7: IGBTs and diodes in 2016 BMW i3 Infineon inverter power module.

2016 BMW i3 Motor Design and Functionality Assessments

The BMW i3 motor is contained in its own assembly, as shown in Figure 8(a), and is separately packaged from other power train components. The motor assembly has an overall mass of 42 kg, a published power rating of 125 kW, and torque rating of 250 Nm. An aluminum sheath is shrink-fitted onto the outer diameter of the stator, and the outer surface of the sheath has a spiral channel to form a circulating cooling path with the outer housing. The stator-sheath unit slides relatively easily out of the outer housing and includes large O-rings on each end to form a seal for the water-ethylene glycol coolant. The other housing, which includes one bearing, has a mass of 6.9 kg, and the sheath/flange has a mass of 4.6 kg. The stator steel core, copper, paper, insulation, and thread have combined a mass of 20.8 kg.

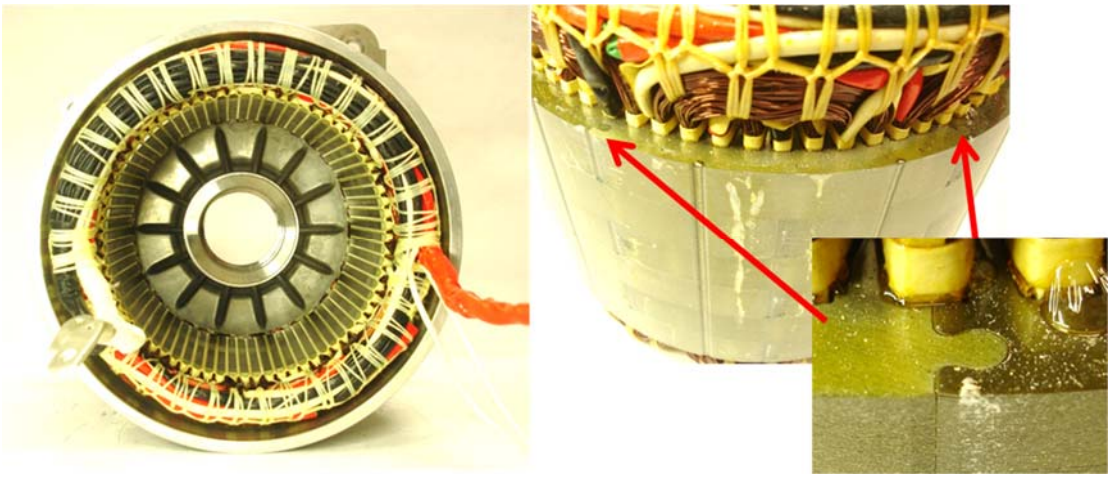


(a) (b)

Figure 8: 2016 BMW i3 motor assembly (a) and motor assembly with outer case removed (b).

Figure 9 shows the stator winding and lamination in more detail. With 72 stator teeth, the machine has 12 poles and six slots per pole. The winding is full pitch and concentrically wound with 12 wires (21 AWG) in hand. Each pole is wired in parallel, giving six parallel paths and nine turns per slot. Two temperature sensors are mounted in the assembly, with one placed on the end turns and one placed near the rotor bearing. In Figure 9(b), it can be seen that the stator laminations are actually composed of six separate sections around the stator joined by what resembles a puzzle piece. This technique can greatly reduce manufacturing waste, as conventional full cylindrical stampings have considerable waste both outside and inside the cylinder, whereas the segmented stator pieces can be stamped in any orientation. The seam at which the puzzle-like interface occurs is alternated in six sections throughout the stack, which is likely to distribute the negative magnetic

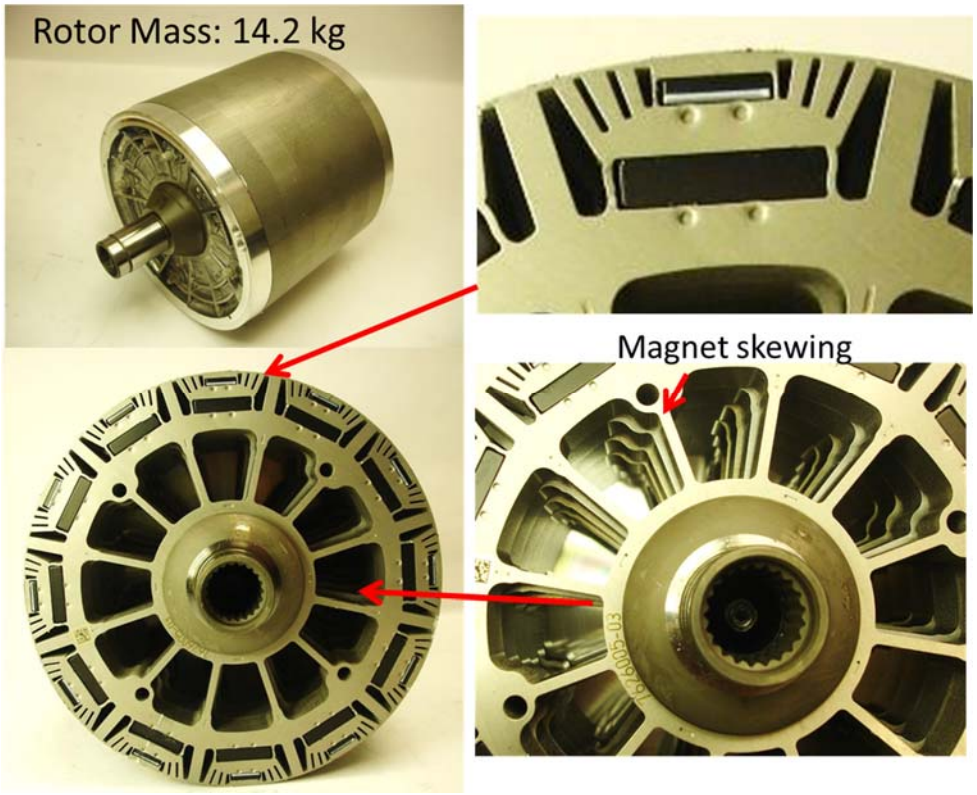
impacts of the seams across multiple phases and poles. The overall core length is 132.3 mm with an OD of 242.1 mm.



(a) (b)

Figure 9: 2016 BMW i3 motor stator front view (a) and stator windings/laminations (b).

The rotor, shown in Figure 10(a), has a total mass of 14.2 kg, which includes the rotor shaft, end plates, end plate bolts, laminations, and magnets. With an outer diameter of 178.60 mm, the lamination design resembles a synchronous reluctance rotor but has one small and one large neodymium iron boron magnet per pole. Incremental magnet skewing, visible in 10(b), is implemented six times throughout the stack, which is likely to mitigate cogging torque and torque ripple during operation. A summary of motor design specifications is provided in Table 1.



(a) (b)

Figure 10: 2016 BMW i3 motor rotor (a) and rotor magnets (b).

Table 1: Motor design specifications

Parameter	BMW i3
Stator OD, cm	24.2
Stator ID, cm	18.0
Stator stack length, cm	13.2
Stator mass, kg	20.2
Stator core mass, kg	13.7
Stator copper mass, kg	7.1
Number of stator slots	72
Stator turns per coil	9
Parallel circuits per phase	6
Coils in series per phase	1 per leg
Number of wires in parallel	12
Wire size, AWG	21
Winding notes	Full pitch, concentrically wound

Dynamometer Evaluation of the 2016 BMW i3 Motor and Inverter

For detailed component testing at ORNL, designs were developed to provide access to the electric motor shaft while maintaining the cooling and lubrication functionality used in the original form. This integration requires special attention to detail because high speed and power levels are involved. A custom plate was designed with high tolerance alignment features and considerations for lubrication. A unique adapter shaft also was designed to adapt the motor shaft to ORNL's dynamometer as shown in Figure 11.

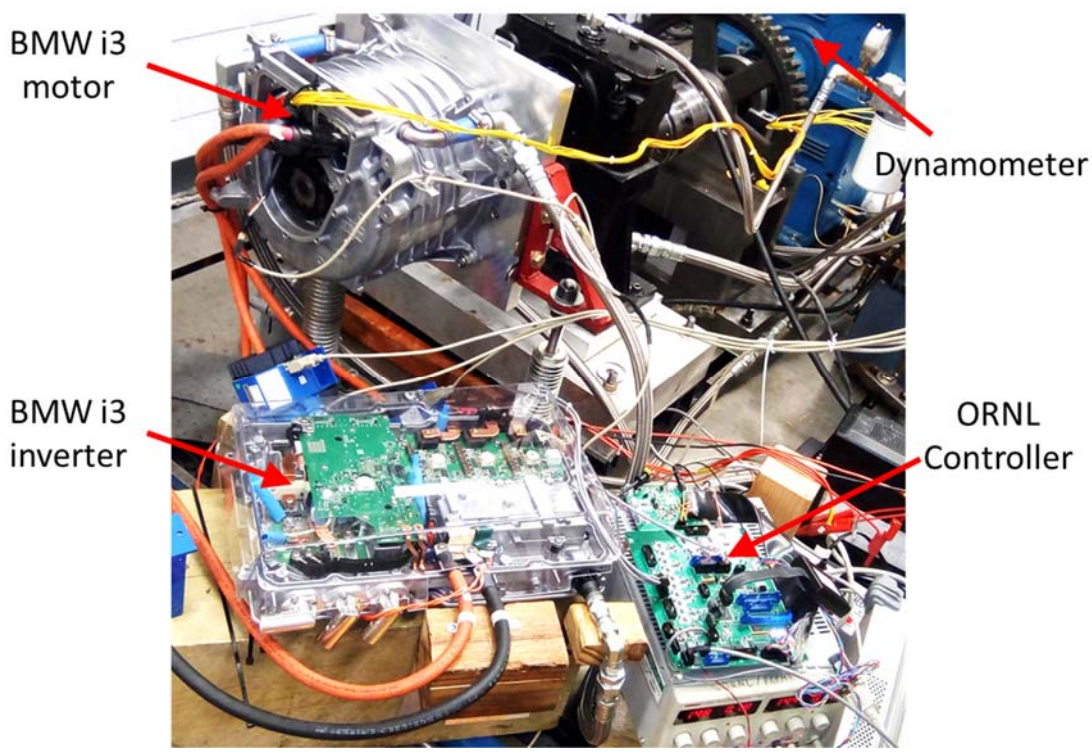


Figure 11: 2016 BMW i3 motor and inverter installed in ORNL dynamometer test cell.

Locked Rotor Tests

The graph in Figure 12 shows locked rotor torque measurements for various positions and applied current. Test results indicate that a peak current of ~530 Adc is required to produce the published peak torque of 250 Nm. Overall, the torque behavior versus position is very smooth, with maximum torque at high currents occurring at about 135 degrees. Linear behavior in the plot of peak locked rotor torque (of all positions) versus current shown in Figure 13 indicates that very little if any magnetic saturation is encountered, even at the published peak torque of 250 Nm.

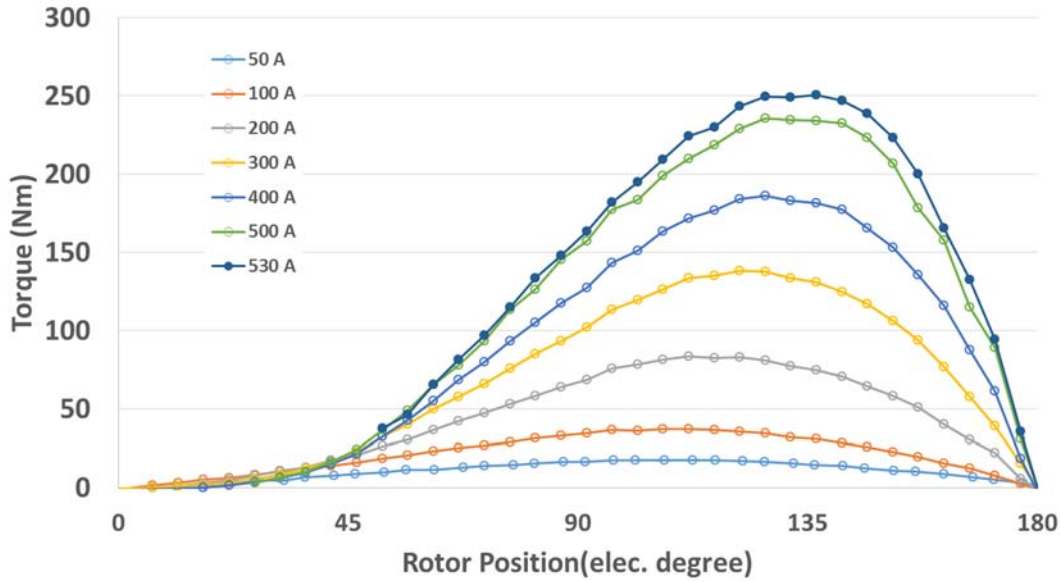


Figure 12: 2016 BMW i3 motor locked rotor torque versus position for various dc levels.

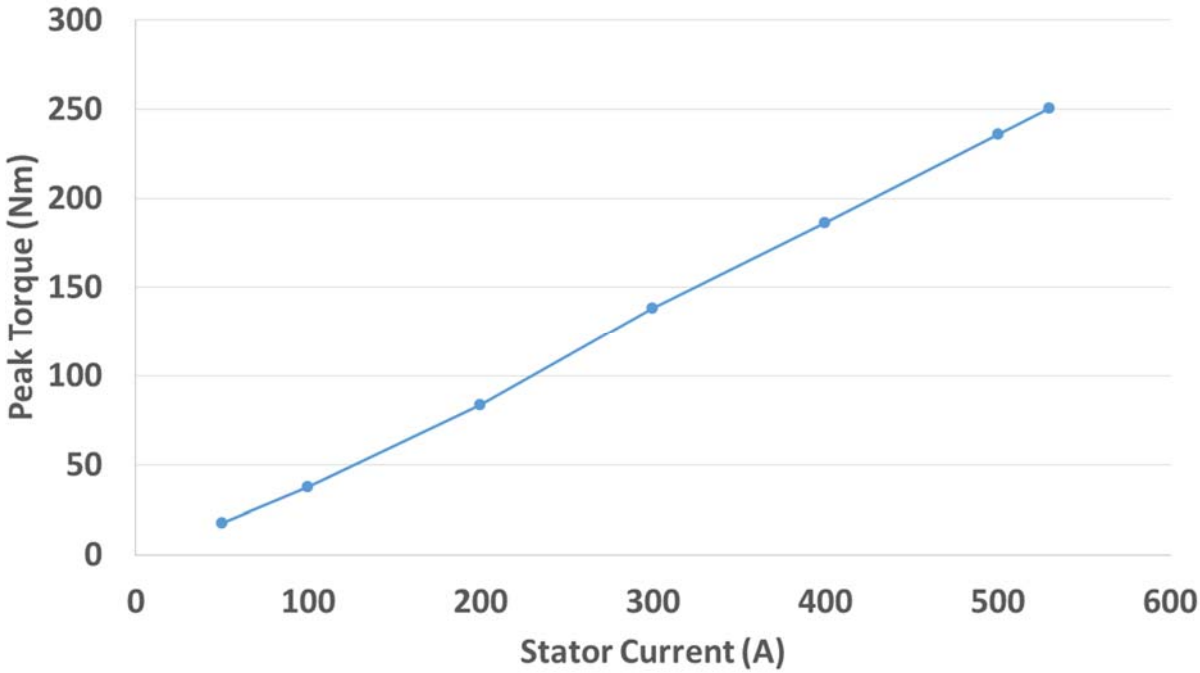


Figure 13: 2016 BMW i3 motor peak locked rotor torque versus position.

Efficiency Mapping, Performance, and Continuous Testing

Performance testing and efficiency mapping for the 2016 BMW i3 was conducted at various torques and speeds for a dc link voltage level of about 360 Vdc. During these tests, the BMW i3 inverter and motor were operated together, as optimal operation at each point was ensured. The inverter was cooled directly with standard automotive 50% water/50% ethylene glycol coolant flowing at a rate of 10 L/min with an inlet temperature of 65°C. Figure 14 shows motor efficiency contours exceeding 94% between ~2,500 and 9,000 rpm at most torques above 125 Nm. Figure 15 shows inverter efficiency contours, with efficiencies ranging from ~88% to 99% as speed increases. As shown in the combined efficiency map in Figure 16, combined motor and inverter efficiencies exceed 90% when the motor operates above torque levels of ~50 Nm at speeds greater than 5,000 rpm. During these tests, the published rated torque of 250 Nm was confirmed at up to a speed of 4,000 rpm. Tests also confirmed that the motor is capable of producing the published peak power of 125 kW at speeds between ~5,000 rpm and the maximum speed rating of 11,400 rpm.

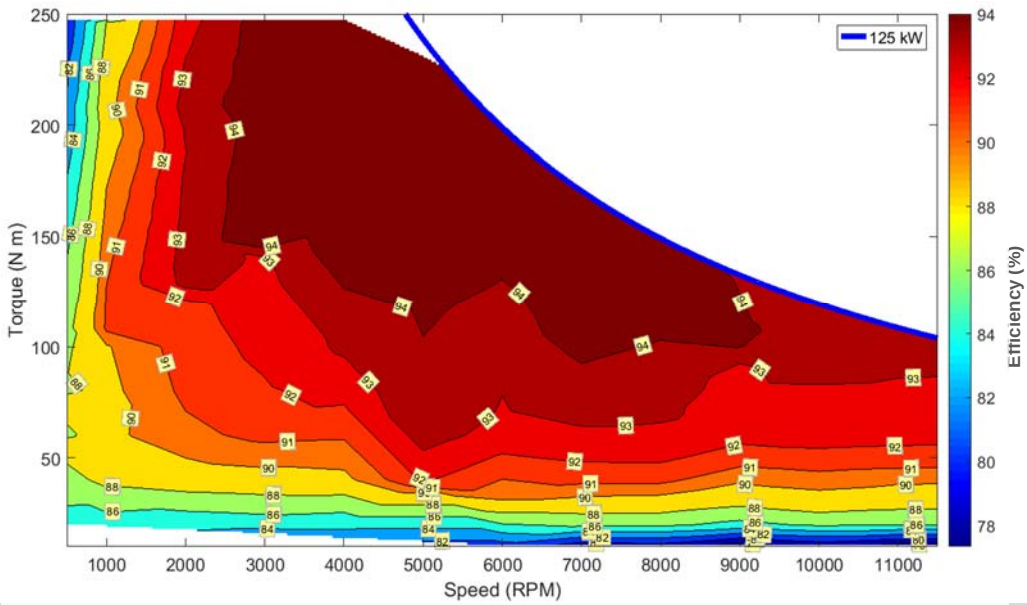


Figure 14: 2016 BMW i3 motor efficiency map.

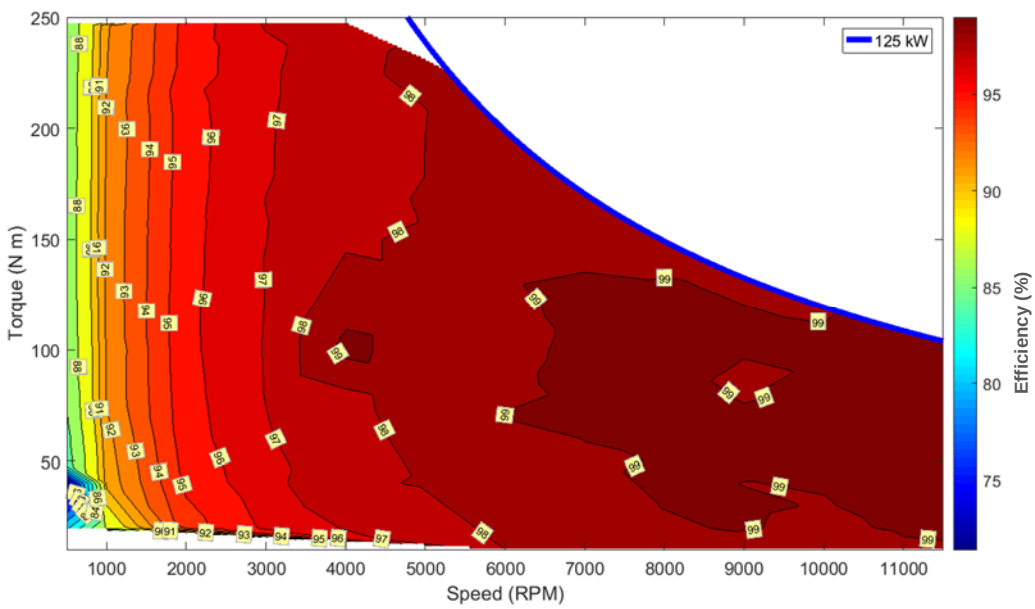


Figure 15: 2016 BMW i3 inverter efficiency map.

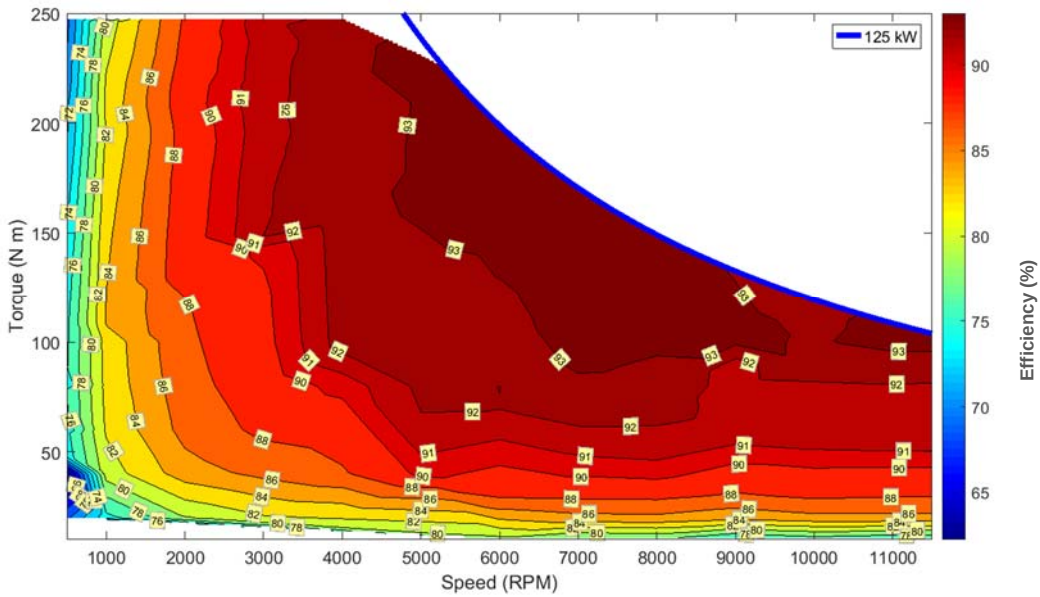


Figure 16: 2016 BMW i3 motor/inverter combined efficiency map.

When possible, continuous tests were conducted at 5,000, 7,000, and 9,000 rpm at power levels of 25, 50, and 75 kW. The plot in Figure 17 indicates the power level and motor winding temperature versus time for continuous tests at 7,000 rpm and 25, 50, and 75 kW. After operation at 25 kW for a half hour, the motor temperature reached about 85°C. Then the power was increased to 50 kW for a half hour, and the motor temperature was relatively stable at ~95°C. Furthermore, the power was increased to 75 kW, and temperatures remained below 110°C. As shown in Figure 18, for continuous operation at 5,000 rpm, motor temperatures stabilized at about 100°C after a half hour of operation at 50 kW.

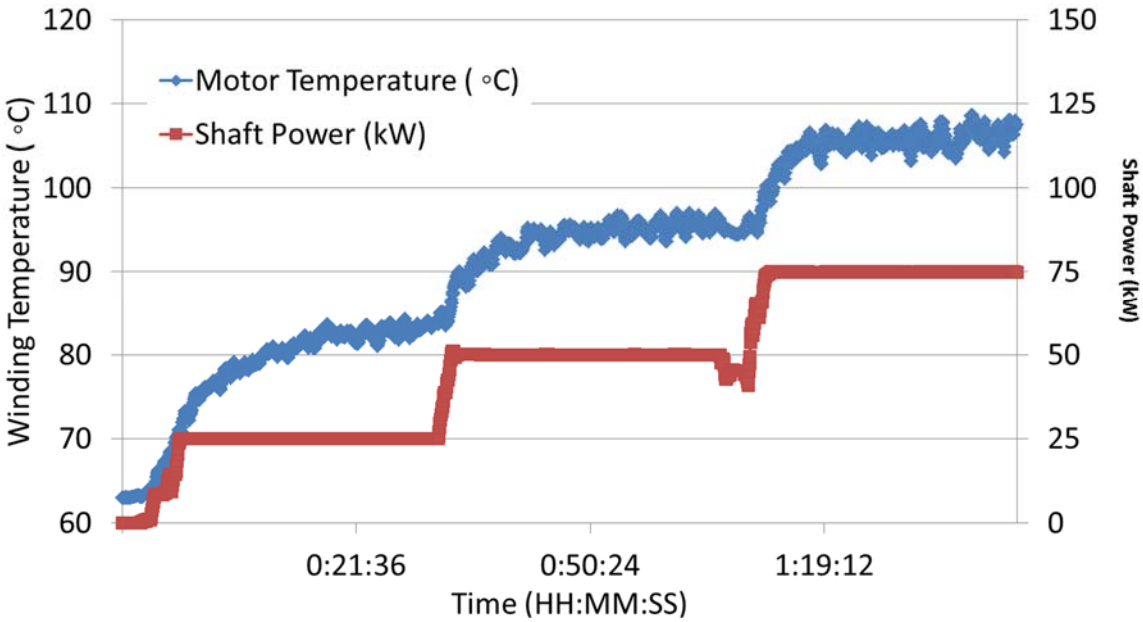


Figure 17: Continuous tests of 2016 BMW i3 motor and inverter at 7,000 rpm and various power levels.

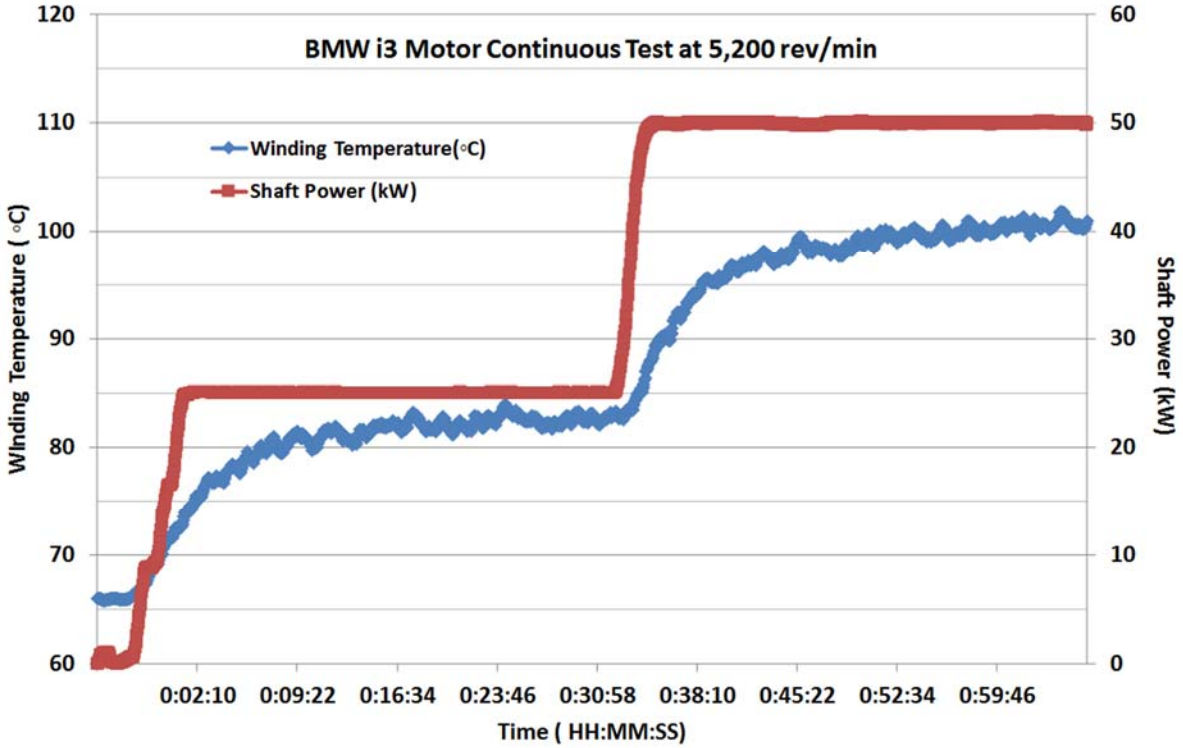


Figure 18: Continuous tests of 2016 BMW i3 motor and inverter at 5,000 rpm and various power levels.

Conclusions and Future Directions

Detailed disassembly and analysis of the BMW i3 inverter assembly revealed key design features, including a commercially available Infineon power module rated for 650 Vdc and 800 A/1,600 A-peak. The 450 Vdc, 475 µF capacitor is very small for the given power rating of the drive system; it is likely that either another capacitor is attached to the dc link or ripple mitigation switching methods are used.

Electric motor teardown analyses yielded many interesting design features, including a shrink-fit water jacket with spiraling cooling channels. A unique approach was taken with the stator laminations to reduce manufacturing waste, as separate pieces were stamped and pieced together with seams that resemble puzzle piece interfaces. The rotor design closely resembles a synchronous reluctance pattern but includes one small and one large neodymium iron boron magnet per pole. There are six magnet segments along the axial length of the rotor that are likely to mitigate cogging torque and torque ripple.

Locked rotor torque tests indicate very smooth behavior of torque versus speed, and it can be concluded that very little or no magnetic saturation occurs, even for the published peak torque rating of 250 Nm. Operation at published peak torque was confirmed up to 3,000 rpm, and peak power of 125 kW was confirmed between ~5,500 rpm and the maximum published speed of 11,400 rpm. Peak motor efficiencies reached 94% for a very wide range of operation, and inverter-motor efficiencies reached 94% for a small region of operation near 4,000 and 5,000 rpm and for torque above 150 Nm. Continuous tests indicated that the system is capable of operating continuously at 75 kW and 7,000 rpm, and the motor temperature remained below 110°C after 30 minutes of operation. During testing at 5,000 rpm and 50 kW, temperatures reached above 100°C after 30 minutes of operation.

Components for the 2017 Toyota Prius will be the focus of FY 2017 efforts. Comprehensive benchmarking of a Toyota product has not been conducted since the 2010 Prius, and there is a high level of interest in these components of this hybrid drive system.

FY 2016 Presentations/Publications/Patents

1. T. Burress, et al., "Status and trends of electric drive technologies," presented at the DOE Vehicle Technologies Program Electric Drive Technologies Electrical and Electronics Technical Team meeting, December 2016, Southfield, Michigan.
2. T. Burress, et al., "Benchmarking EV and HEV technologies," presented at the DOE Vehicle Technologies Office 2016 Annual Merit Review, June 2016, Washington, DC.

5.1 Advanced Packaging Technologies and Designs

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Contractor: UT-Battelle, LLC, managing and operating contractor for ORNL
Contract No.: DE-AC05-00OR22725

Abstract/Executive Summary

- The project was focused on the development and implementation of advanced packaging technologies for wide bandgap (WBG) semiconductor power modules to accelerate the application of WBG power semiconductor devices in the automotive industry.
- Specific packaging technologies were designed and developed for in-house manufacture of the WBG power modules for automotive inverters and converters, using the latest industrial WBG devices and integrating electrical, thermal, and mechanical functions in a high-density package.
- Innovative packaging technologies and designs were developed for using superior attributes of the WBG devices. The simulations and experimental analyses were performed and validated the advances of the design and technologies. The packaging process development leads to improved manufacturability and high reliability. The in-house-fabricated prototypes successfully demonstrated the advances of the WBG power electronics packages.
- Commercial state-of-the-art silicon carbide (SiC) power modules were analyzed and their limitations examined.
- Working jointly with other projects within the program for development of the systemic power electronics packaging, prototypes for thermal analysis were made and delivered.
- New bond materials and processes were developed and implemented in the SiC modules for advancing power electronics materials research.
- One patent application and one invention disclosure were filed in addition to five publications.

Accomplishments

- Developed a packaging approach of multiple chip-scale packaged gallium nitride (GaN) devices for high mechanical flatness, enabling three-dimensional (3-D) high density assembly. Fabricated and delivered GaN modules for building a 6.6 kW GaN isolation converter in project EDT 054.
- Performed electromagnetic simulation and experimental evaluation of state-of-the-art commercial power modules. Electrical performance limitations of the module packaging have been identified. Technical aspects for further improvements have been suggested.
- Designed and fabricated record-low switching ringing SiC modules. A feature inductance of 1.46 nH in a SiC power module has been realized for the first time. This will allow converter/inverter

operation at higher frequencies and low electromagnetic interference (EMI) and, in turn, lower cost and high power density.

- Developed large area bonding process technologies for high reliability SiC modules. New materials and processes push SiC operating temperatures higher and increase the reliability by 3 times.
- Fabricated and delivered SiC planar-bond-all modules to the National Renewable Energy Laboratory team for thermal evaluation. The double-sided larger area bonds increase the area of the thermal path by 40%, allowing reduction of thermal resistance and reduction in cost and increase in power density.
- Established a power cycling method and test bed for power cycling tests of WBG module packaging.

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Introduction

Existing automotive inverter designs with silicon power semiconductor modules will likely not meet the DOE EDT 2022 cost, size, and efficiency targets. State-of-the-art power inverters and converters in electric vehicles (EVs) are manufactured by using conventional packaging technologies; however, the electrical, thermal, and thermomechanical performance of these inverters, as well as their manufacturability, is limited. These limitations cause large power losses, low semiconductor operational temperatures (limited to 150°C), high thermal resistance (0.6 $cm^2 \cdot °C/W$), and poor power thermal/temperature cycling capabilities, resulting in low efficiency and high costs.

WBG semiconductors such as SiC and GaN permit devices to operate at much higher temperatures, currents/voltages, and frequencies—making power electronic systems using these materials significantly more powerful and energy efficient than ones made of silicon. They also offer greater efficiency in converting electrical power and operating electric traction drives.

The objective of this project is to address the challenges and barriers to use of WBG technologies for automotive electric drives. This research will develop WBG automotive power modules in inverters/converters through advanced packaging to accelerate their adoption in traction drive systems and achieve the potential superior attributes of WBG power semiconductors: high current density and low losses, fast switching, high temperature operation, etc.

This research will lead to all-inclusive improvements in the performance and manufacturing of power modules for use in inverters/converters as a result of transitioning from silicon to WBG power semiconductors and of innovations in packaging materials, structure, and processing. These comprehensive advances can directly affect the cost, efficiency, reliability, and density of power electronics systems in the electric drives of EVs. The goal of a 40% cost reduction and 60% power density increase in the power module supports DOE EDT 2022 power electronics targets of $3.3/kW and 14.1kW/kg, respectively.

Approach

- Realize the targets of cost reduction, power density increase, and power efficiency improvement through leapfrogging barriers of the existing industrial baseline and bringing innovative, systemic development by advancing technologies that improve technical metrics: thermal resistance (θja), parasitic electrical impedance (Lp, Rp, Cp), thermal expansion coefficient mismatch (ΔCTE), and manufacturability.
- Evaluate state-of-the-art power module packaging technologies through simulation and experimental measurement to examine limitations of the performance of the module packaging and identify technical aspects for further improvements.
- Fabricate prototypes of the all-WBG power modules for automotive inverters and converters by adopting the latest industrial WBG power semiconductor devices in custom designs to take advantage of the superior attributes of WBG power semiconductors.

- Develop innovative power packaging techniques featuring optimized electrical interconnections, highly efficient heat transfer, multifunctional structural integration, high reliability at high temperature operation, and low cost manufacturing.
- Deliver advanced packaging solutions: optimal packaging designs, data on state-of-the-art packaging technologies, and novel processes for cost-effective manufacture of integrated WBG power electronics systems.

Results and Discussion

The development and evaluation of advanced WBG packaging technologies are summarized in the following four sections: GaN power module packaging for charger inverter, evaluation of state-of-the-art power module packaging, ultralow inductance SiC power module packaging, and high reliability packaging technologies. Performance improvements were determined mostly through experimental measurements and simulations, and efficiency, cost, and reliability benefits to power electronics systems were evaluated.

A. Gallium Nitride Power Module Packaging for Charger Inverter

A customized GaN power module was developed as part of another project, EDT 054 (WBG chargers R&D). This all-GaN power module is composed of the latest GaN metal oxide semiconductor field-effect transistors (MOSFETs). The switch units consist of up to three paralleled MOSFETs, and the two coupled H-bridge modules include a maximum 24 devices. The selected GaN MOSFET is chip-scale packaged (the MOSFET die is embedded in the plastic resin case with double-sided metal pads on the planar surfaces). A thermal pad is on the top surface while electrodes [source (S), gate (G), and drain (D)] are all on the bottom side. The dimensions of the package are 9.00 mm (L) × 7.65 mm (W) × 0.54 mm (H). In the packaging design of this all-GaN power converter module, two printed circuit boards (PCBs) are used to bear all the GaN MOSFETs and provide electrical interconnections. Solder bonds join the devices to the board underneath each electrode pad. The other surfaces of the PCBs are designed for assembly of other electronic components. Then the two boards are attached to a liquid-cooled heatsink through tight contacted thermal interface material.

The challenges for packaging of the GaN MOSFETS on board include (1) flip-chip soldering of multiple chip-scale device attachments on the circuitry, (2) alignment of multiple devices to pads on the PCBs, (3) flatness of the multiple devices for attachment to the cold plate, and (4) uniformity in electrical performance of paralleled devices.

For better paralleling, the devices have been sorted based on their electrical performance using a special fixture made in house. Figure 1, a photo of the final assembly of multiple devices and PCB board on a hot plate for reflow soldering, displays some of the techniques taken to overcome the difficulties mentioned above. A special mask was designed and fabricated for alignment of multiple devices and pads on the PCBs; it also withstands the soldering temperature (240ºC) and allows placement of a flat cover and weight on top of these thin devices during solder reflow. The assembly is located on the hot plate in an environment-controlled oven to avoid solder defects. A number of GaN power modules for charger converters have been fabricated at the ORNL packaging laboratory with these measures. Figure 2 shows two packaged GaN power units (eight MOSFETs each). The power devices are packaged separately on two PCB boards for the upper unit and lower unit in converter assembly. The packages, which meet the design specifications, have been delivered for further testing in the GaN charger prototypes.

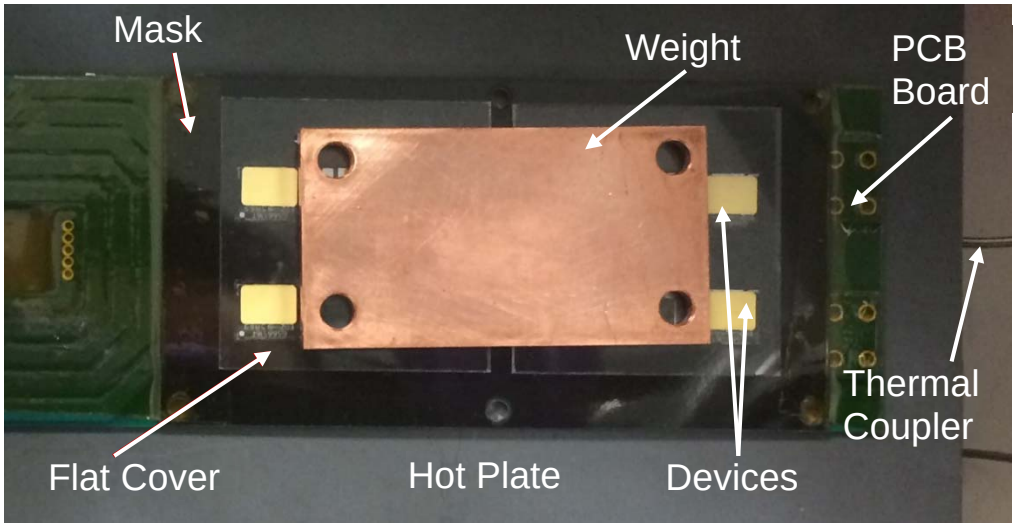


Figure 1: Photo of the final assembly of all parts for soldering multiple GaN MOSFETS (devices) on a PCB board on a hot plate in a solder reflow oven to form a power module.

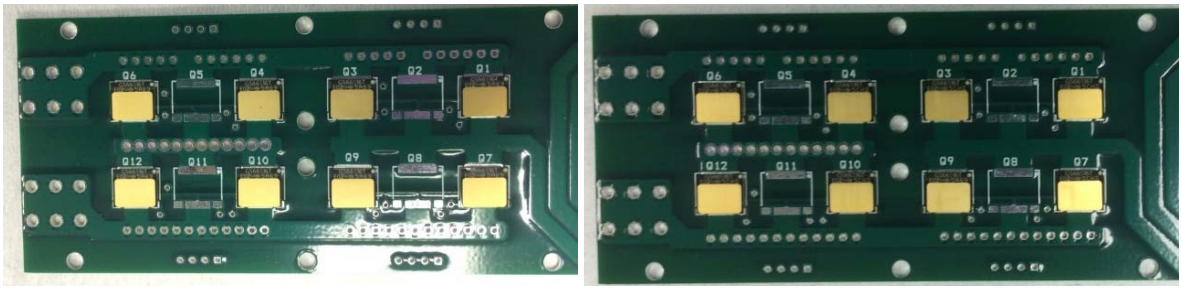


Figure 2: Two packaged GaN MOSFET power phase legs (eight MOSFETS each) for assembly of a GaN charger converter (project EDT 054).

B. Evaluation of State-of-the-Art Power Module Packaging

The power converters and inverters are made in different topologies through electrical interconnection of multiple power semiconductor devices by packaging processes. These interconnections, made of electrical conductive materials, bring parasitic electric impedance to the pure semiconductor circuits. The parasitic components have severe effects on switching performance of the power semiconductor devices, leading to large, high-frequency electric spike and ringing during switching transitions. The electric parasitic parameters are among the critical technical metrics used to evaluate and compare packaging technologies. For this study, the power module in a 2013 Toyota Camry Hybrid electric drive system was examined. Figure 3(a) is a photo of the unit modules (paralleled insulated gate bipolar transistor and diode) that, when assembled, make a half-bridge, like overlaid electric diagrams. Multiple half-bridge assemblies, which are double-sided cooled by stacked coolers, are electrically interconnected through a bulky copper frame, as shown in Figure 3(b). Figure 3(c) illustrates the 3-D model of the modules and interconnections in the assembly. The parasitic impedance is modeled as a lumped element associated with each interconnection section, shown as the electric diagram in Figure 3(d). The values of each element were calculated based on the geometry of the electrical interconnection and material properties using electromagnetic simulation software (Ansys Q3D Extractor). It is well known that the inductances, along with the major power commutation loops, CL1 and CL2 in Figure 3(d), are the most critical ones for power conversion performance of the inverters and converters. The calculated commutation loop inductance is about 63 nH. It is worth noting that the planar modules themselves offer very small inductance; however, the complex terminals produce much larger inductances (Lp and Ln) than conventional wire bond modules (generally around 35 nH). This can be concluded as one of the major drawbacks of such packages.

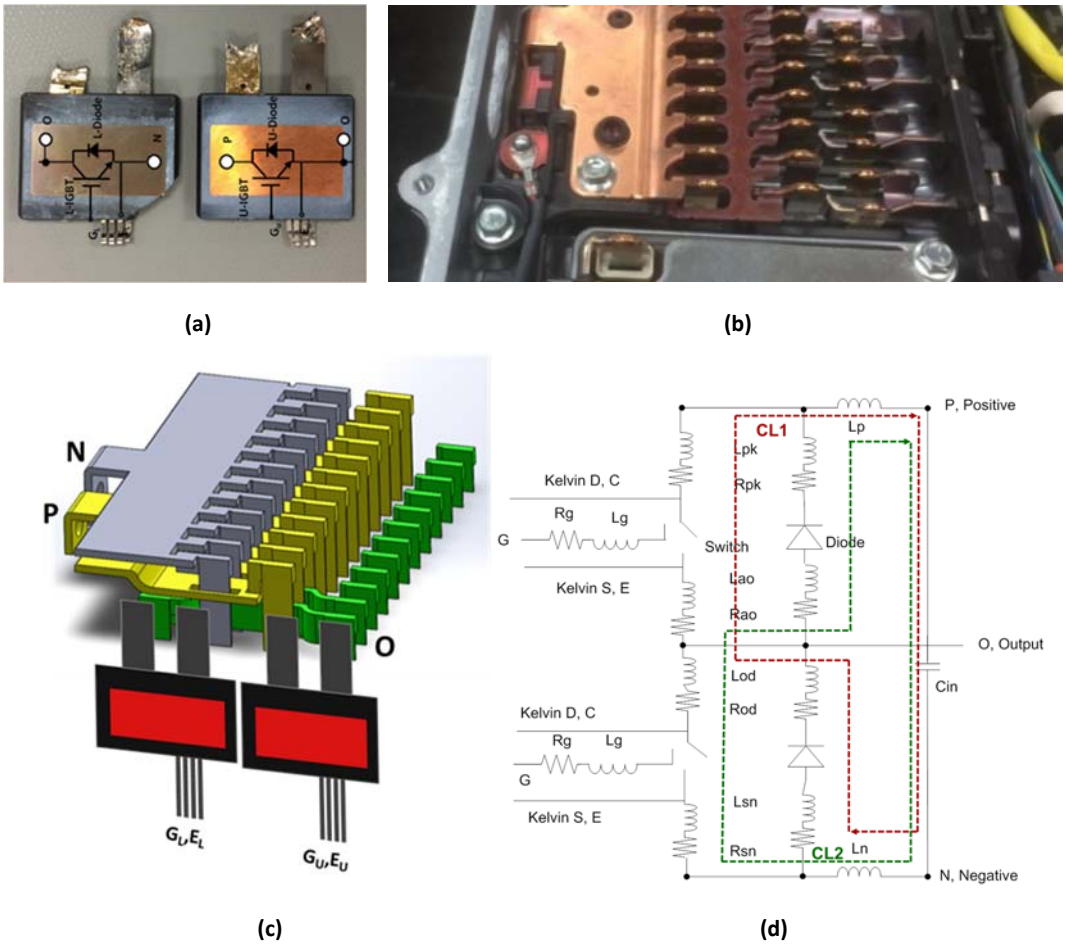


Figure 3: Analysis of parasitic inductance in the 2013 Toyota Camry inverter: (a) planar power modules with overlaid electric diagrams, (b) photo of partial inverter with copper terminals, (c) 3-D model of the electrical interconnection in inverter module, and (d) lumped element model of parasitic electric components with illustrated major power commutation loops.

Another evaluation was performed experimentally on a state-of-the-art SiC module, as shown in Figure 4. An all-SiC half-bridge module made of CREE's C2M MOSFET (1.2 kV, 13 mΩ) and Z-Rec Diode, is assembled on a specifically designed and fabricated test bed optimized with electrical interconnection and with specific instrumented current sensor and voltage test points. A specific gate drive board is also made to closely connect the module with variable gate resistance. The module is mounted onto a hot plate to elevate its temperature.

The MOSFETs' turn-on and turn-off switching were tested under different operation conditions: the bus bar voltage is fixed at 600 V while the current is from 30 to 100 A; the gate resistor (Rg) is from 0 to 20 Ω (with steps of 5 Ω); temperature is from 25°C to 150°C (at 25°C steps). Figures 5(a) and (b) show the waveforms of the current Id, voltages Vds, Vgs at Tj = 150°C with the gate resistance varying from 0 to 20 ohms. The switching parameters such as rising time (tr), falling time (tf), delay times (tds), dV/dt, dI/dt, as well as their dependence on the test conditions can be extracted. Figure 5(c) presents the dV/dt dependences on both Rg and operation temperature. All these data have been collected and represent the characteristics of this SiC product. Extensive comparisons and further analyses of the data have been performed.

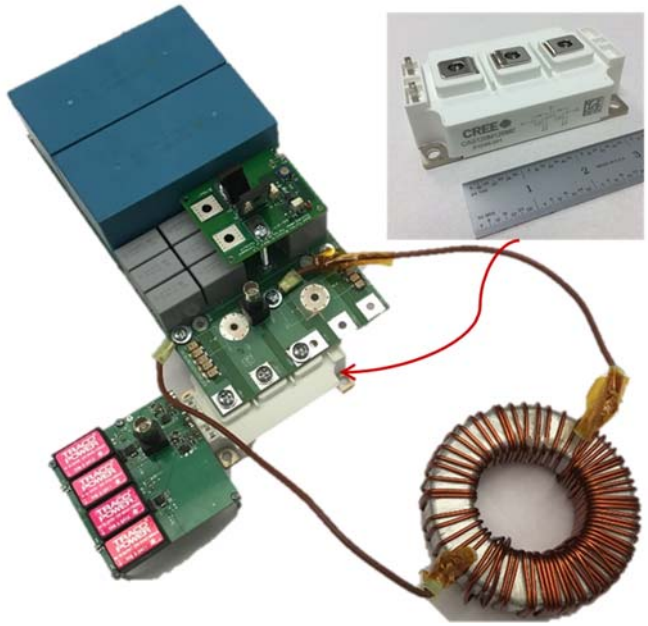
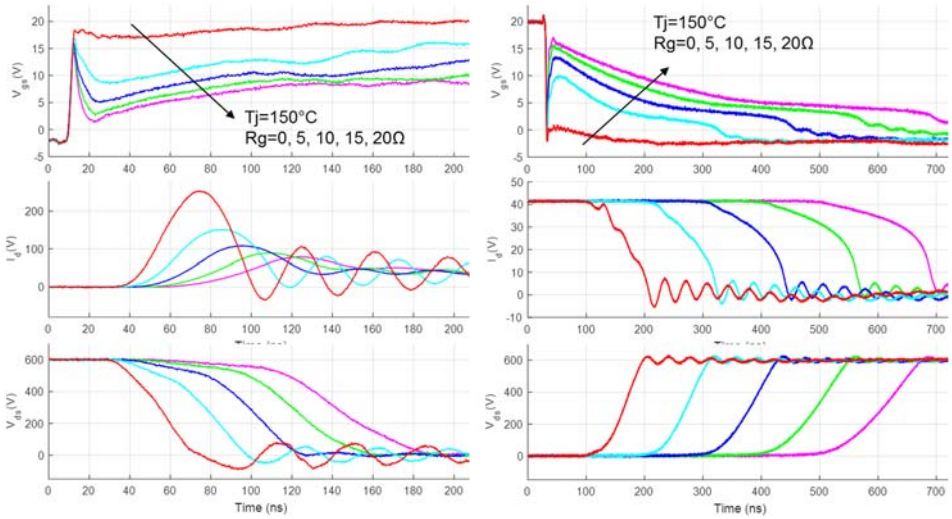
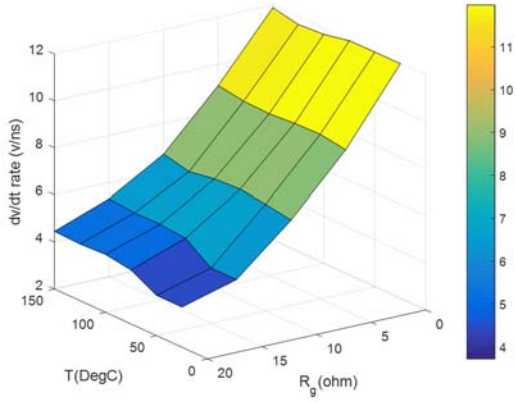


Figure 4: The test setup for evaluation of switching performance of a SiC module: CREE's CAS120M12BM2 (upper right corner).



(a) **(b)**



(c)

Figure 5: Measured switching performance of Cree SiC MOSFET in module CAS120M12BM2: waveforms of the current Id, voltages Vds, Vgs at Tj = 150°C with the gate resistance varying from 0 to 20 Ω [(a) and (b)]; dV/dt dependences on both Rg and operation temperature (c).

C. Ultralow Inductance SiC Power Module Packaging

As discussed above, the parasitic inductances within the module package more severely affect the switching performance of fast devices such SiC and GaN. Therefore, it is important to develop packages for the WBG modules with smaller moderate parasitic inductance, thus ensuring high performance, safe operation of these devices.

Figure 6 presents the design and development of an all-SiC half-bridge power module with ultralow inductance. Figure 6(a) shows its electric diagram, with two SiC MOSFET dies and two SiC diode dies paralleled as a switch unit to form a 100 A, 1,200 V SiC phase-leg. Except for power connectors, P, O, and N terminators, the so called Kelvin gate, source and drain pins are added for separation of power loops and drive (signal) loops, which will greatly reduce the electric coupling between them. Figure 6(b) presents an aerial view of the designed package with the planar interconnection configuration. Between two direct bond copper (DBC) substrates, the two upper MOSFETs and two lower diodes are arranged on the left lower half of the package and two lower MOSFETs and two upper diodes are placed on another half of the substrate so that the commutation loops CL1 and CL2 are located in a smaller space with the shortest distance, as depicted in Figure 6(a).

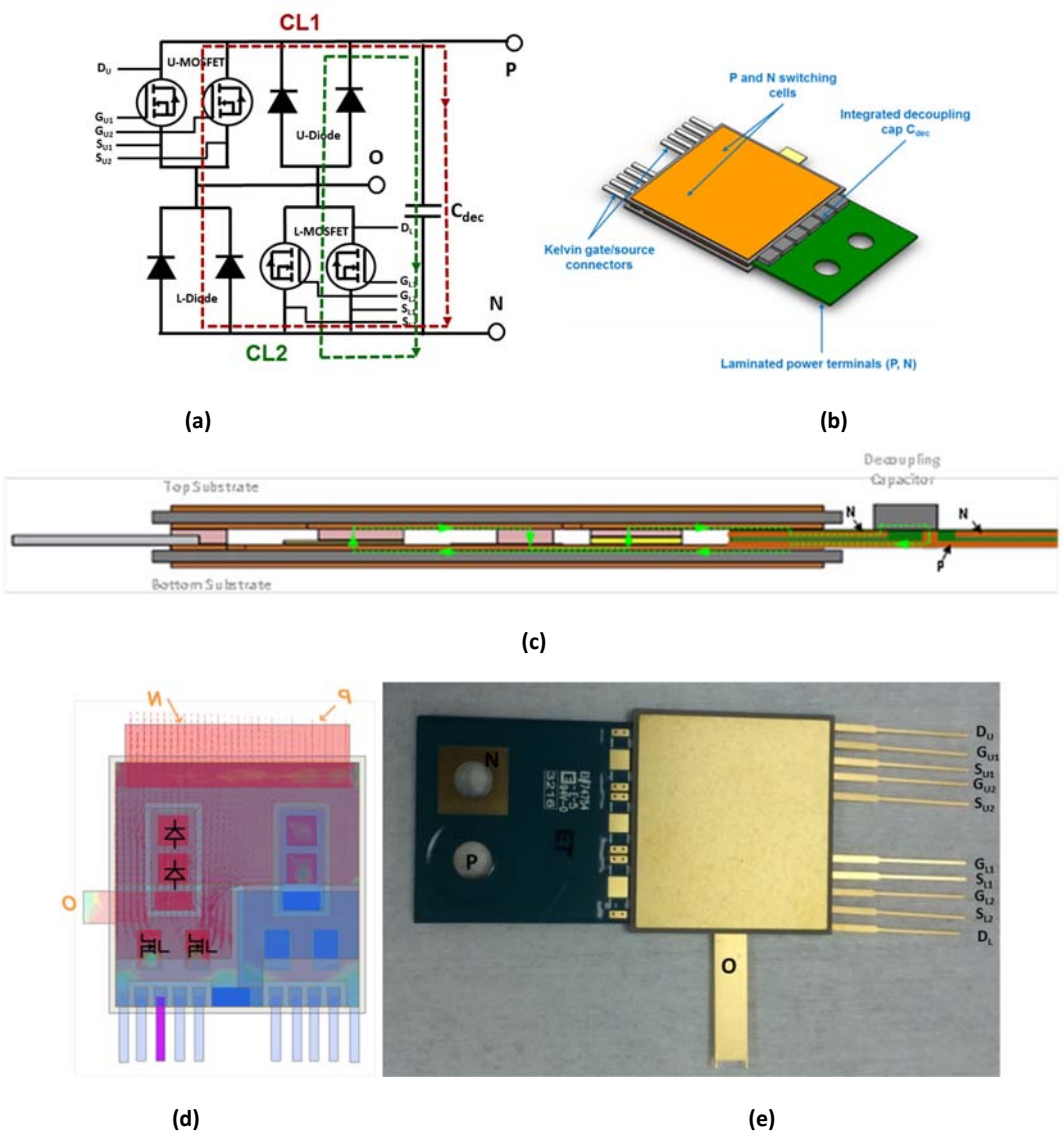


Figure 6: Design of an ultralow inductance SiC phase-leg module: (a) electric diagram with regrouped switches; (b) aerial view of the planar package; (c) cross-sectional view of the interconnections and current in commutation loop; (d) current density distribution in the package along a commutation loop; and (e) photo of laminated planar-bond-all package of a 100 A, 1,200 V SiC MOSFET/JBS diode phase-leg power module.

In the package all dies are directly bonded onto the top and bottom substrate by solders. The top and bottom substrates have patterns (such as copper traces) on their inner surfaces for electrical interconnection. The metal shims (spacers) are used to connect the pads on the top and bottom substrates. The signal pins (Ss, Ds, Gs), are arranged on the left side with bond wire connections with the MOSFETs, while the power terminals (P, N) are made of laminated two-layer copper conductors and can be directly mounted between the top and bottom substrates and bonded onto their inner surfaces. The power output pin O is also bonded on the bottom substrate. The laminated P and N terminals provide a "friendly" interface for connection to the capacitor tank of the inverter, leading to tremendous reduction of the stay inductance with the power bus bar compared to that in Figure 3(b). The so-called decoupling caps are integrated (mounted) on the P and N terminals, which are designed to compensate for the inductive effects and effectively constrain electric ringing during device switching.

Figure 6(c) illustrates the cross-sectional view of a commutation loop. It can be seen that the power terminals P and N are fully and closely laminated. This laminated electric conduction configuration not only shortens the power flowing distance in the package, but also makes use of the electromagnetic cancellation effect to reduce parasitic inductance along the loop. In addition, the decoupling caps are so closely mounted to the devices that the CL1 and CL2 loops can be very small.

Figure 6(d) shows the current density distribution during electric power flow along the CL1 loop. It can be seen that the gap between current paths in different directions will offer strong coupling. The final extracted parasitic inductance, by Ansys Q3D Extractor, is 1.46 nH, much smaller than the 35 nH of conventional wire bond modules.

Figure 6(e) is a photo of the 100 A, 1,200 V SiC phase leg power module prototype fabricated from this design. All eight SiC dies were bonded between two DBC substrates by solder from both the top and bottom surfaces [see Figure 6(c)]. At the same time, the laminated power terminals P and N (on the left side) and O (on the bottom side) and signal pins Gs, Ss, Ds, are also mounted onto the DBC substrates. A soldering process was used to form the planar bonds. It offers high electrical conductivity and easy processing. The final package dimension is 40 × 37 × 2 mm, excluding the terminals and pins.

The parasitic inductance was measured using a specially built power switching test system to experimentally test electrical performance of the devices in the package. Figure 7(a) is a photo of the experimental setup with the module connected to the power stage and gate drive board. Figure 7(b) illustrates the electric diagram of this test circuit. With fixed bus bar voltage, the gate drive supplies two continuous pulses (from −2 V to 15 V) to the MOSFET, adjusts the widths of the pulse to the power inductor, and controls the current going through it (load current). Thus, the current and voltage variations during turn-on and turn-off can be picked up through current sensor (shunt) and voltage test points (Bayonet Neill-Concelman connectors) instrumented in the modules and test boards. The parasitic inductance can be extracted simply by the ratio of the overshoot voltage over the current slope (dI_d/dt). Note that the overshoot voltage at different test points is dependent on the sectional inductances included in the test loop. For example, in the graph of Figure 7(c), the overshoot voltage (ΔVpn) of the Vpn (blue) is caused by parasitic inductances Lstray 1 and Lstray 2 [Figure 7(b)], while the voltage Vds (between Kelvin D and S terminals) overshoot (ΔVds) is caused by all elements in the loop, Ld, La, Lk, Lp, Ls, and Ln, in addition to Lstray 1 and Lstray 2. Thus, the module's total internal inductance can be calculated based on the difference between Vds and Vpn. Specifically, the extracted value based on the test in Figure 7(c), is 3 nH. Furthermore, the designed decoupling caps are mounted on the laminated terminals as shown in Figure 6(b), and the voltages Vpn and Vds change greatly as illustrated by the waveforms shown in Figure 7(d). The ringing of Vpn has been completely eliminated. The ringing of Vds has been reduced to only half magnitude. The reason is that the commutation loop has been shrunk to the path formed by internal devices and the decoupling caps (Cdec), excluding effectively the Lp and Ln associated with power terminals. The internal inductance calculated based on this measurement is 1.5 nH, in good agreement with the simulation. This is a record-low value compared to other counterparts.

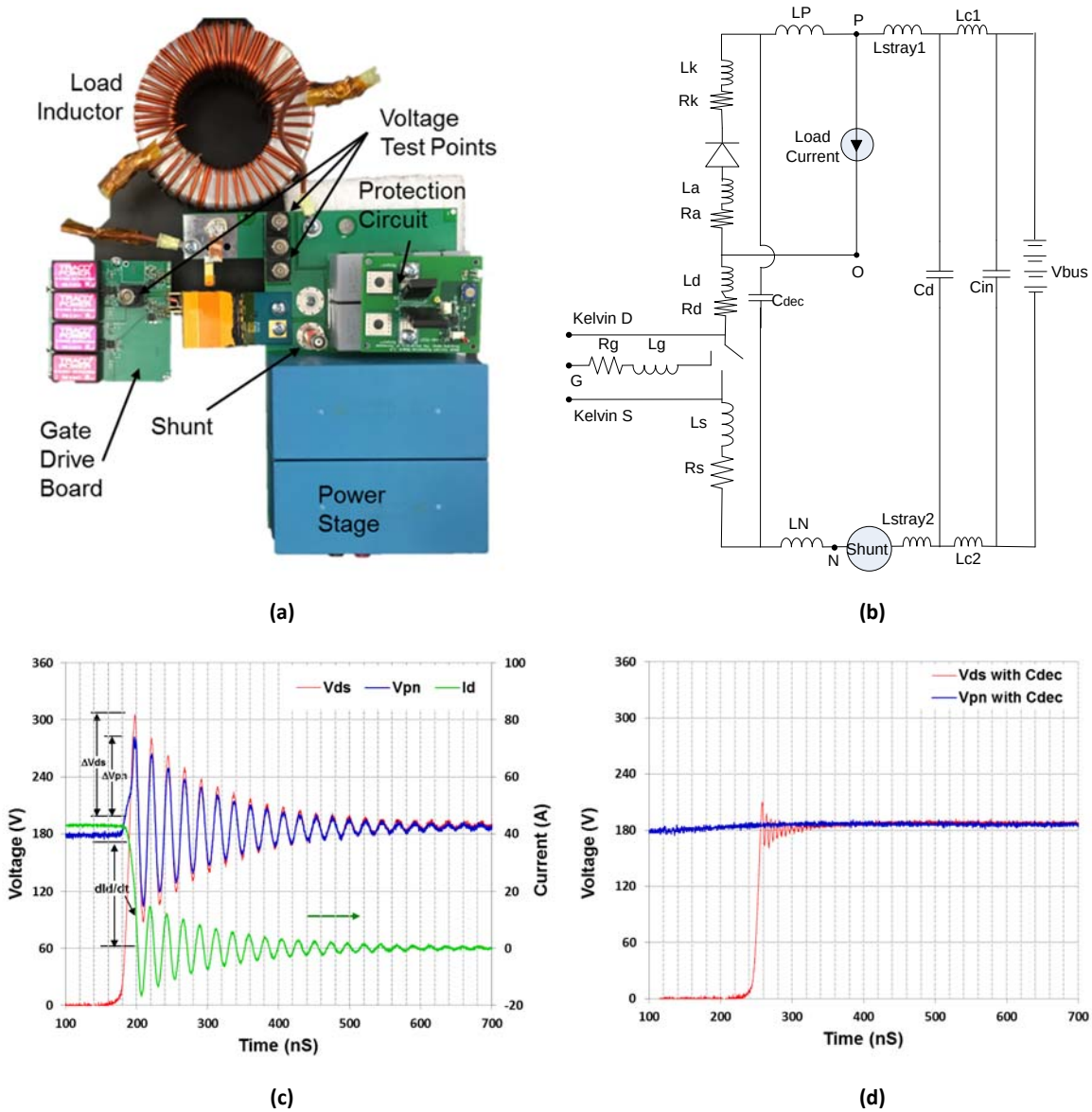
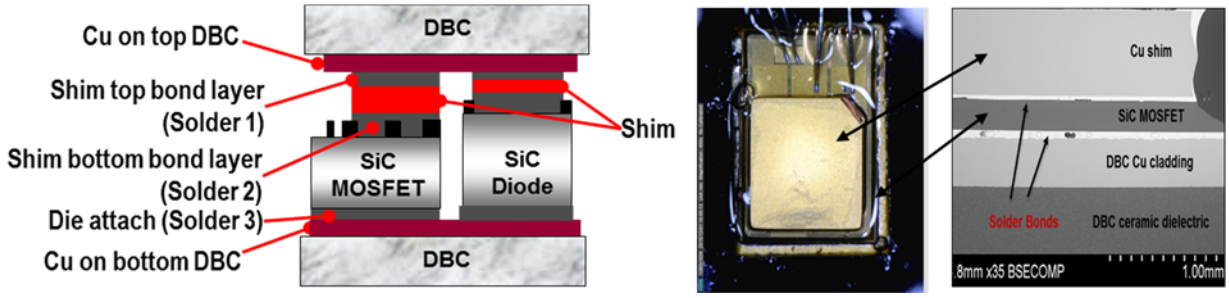


Figure 7: Test of the electrical performance of packaged modules: (a) experiment setup; (b) electric diagram of the test circuit (c) typical waveforms of switch turning off; and (d) waveforms with added decoupling caps.

D. High Reliability Packaging Technologies

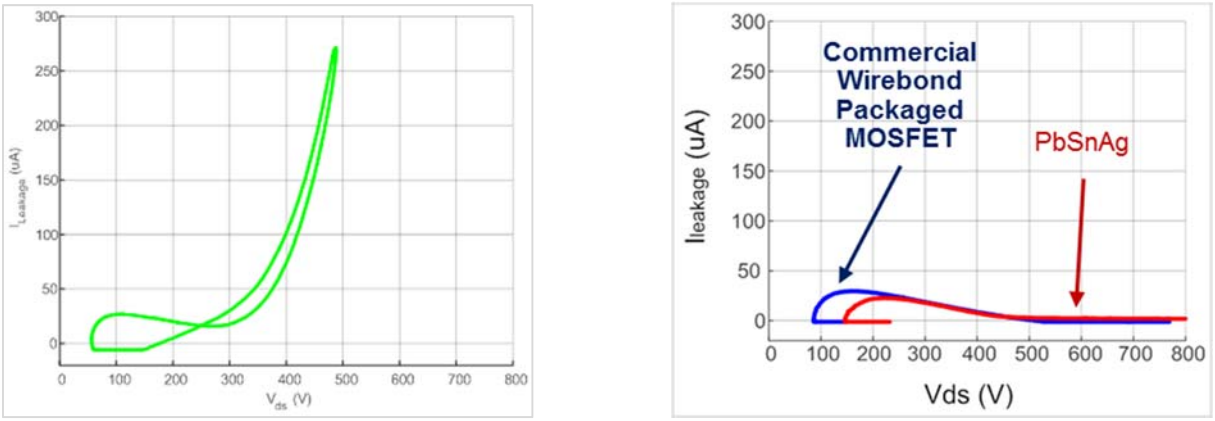
The planar bonding packaging implies that both the tops and bottoms of the device dies are attached to the metal pads (electrically conductive) on the power substrates such as DBCs. Figure 8(a) is a cross-sectional diagram of a SiC MOSFET and a diode in parallel in such a package, where the shims on each die with different thickness are inserted between the top surface and the top substrate, and the whole package is joined together by three-layer solders. The shims compensate for the thickness mismatch among different devices. Figure 8(b) shows photos of a SiC MOSFET die attached on a DBC substrate with a shim bonded on top, while the tiny wires are bonded onto the small gate and source pads for Kelvin connectors.



(a) (b)

Figure 8: Planar bond of SiC dies in package: (a) Cross-sectional view of a SiC die bonded onto a DBC substrate through shims; (b) photos of a shim bonded on SiC MOSFET.

To facilitate the high-temperature operation capability (>200ºC) of the SiC devices, higher melting point solders were chosen for the three-layer bonding. The first tested solder was gold-tin (AuSn), a eutectic alloy with a melting point of 280ºC. However, an unexpected higher leakage current of the SiC MOSFET (at high voltage blocking state) when a copper shim is bonded on top as shown in Figure 9(a), was observed. The normal leakage current of this device is shown in Figure 9(b), which depicts a commercial wire bond packaged MOSFET. This degradation in leakage current was briefly attributed to the residual mechanical stress induced during cooling down of solder reflow due to the large difference in the coefficient of thermal expansion (CTE) between copper and SiC. This conclusion has been indirectly proven by additional experiments. First, a thinner copper shim was used, and the degradation was very minor. Second, the AuSn solder was replaced by a lead-tin-silver (PbSnAg) solder (noneutectic, melting points 287°C–296°C). The leakage current measurement is shown in Figure 9(b), which corresponds well with the wire-bonded one. The reason is that this solder has a modulus of elasticity (Young's modulus) of 13.8 GPa, smaller than the 74 GPa of the AuSn solder; thus it releases the residual stress through its deformation in the final stack. Furthermore, a new alloy (with close CTE, 7 ppm/C to SiC) was used to replace the copper ones in the AuSn solder bonding package, and the degradation of the leakage current was eliminated.



(a) (b)

Figure 9: Leakage current of SiC MOSFET in different packages: (a) AuSn soldered copper shim; (b) wire-bonded package and PbSnAg soldered shim.

As discussed above, although the impacts of the larger area metal attachment on electrical performance were eliminated by changing the materials in the package, the mechanisms behind these phenomena have not been intensively investigated. Further studies on this topic are necessary to fully understand fundamentals related to the reliability of newly developed WBG devices.

Sintered silver layers are well known to be a superior die attachment (bonding) compared to solder layers for WBG power module packaging. It offers much better electrical; thermal; and, especially, thermomechanical properties.

In recent years, intensive research has been conducted on the process technologies for in situ sintering of nano-silver pastes for SiC device packaging. Figure 10 presents some results of this research. Figure 10(a) shows a cross-sectional view photo of a SiC diode die attached to a DBC substrate. A good bond layer was formed between die and substrate by using optimized processing parameters. However, silver outflow from the bond layer was observed. It was the result of a little pressure on the die when it was placed on the wet silver paste before sintering. For improving the accuracy of the die attachment and preventing any potential electrical defaults, a special pro-bake processing was developed that ensures maintaining the printed geometry and realizing successful no-pressure sintering. Figure 10(b) shows a broken interface at the bond layer. Uniform sintered silver residues can be seen on both substrate and die surfaces. Furthermore, as shown in Figure 10(c), three silver layers replace all solder layers [shown in Figure 8(a)] to form a planar package with the SiC diode. Figure 10(d) is a photo of the sheared off shim bottom bond layer (sintered Ag 2) from one of these three-silver-layer bonded packages.

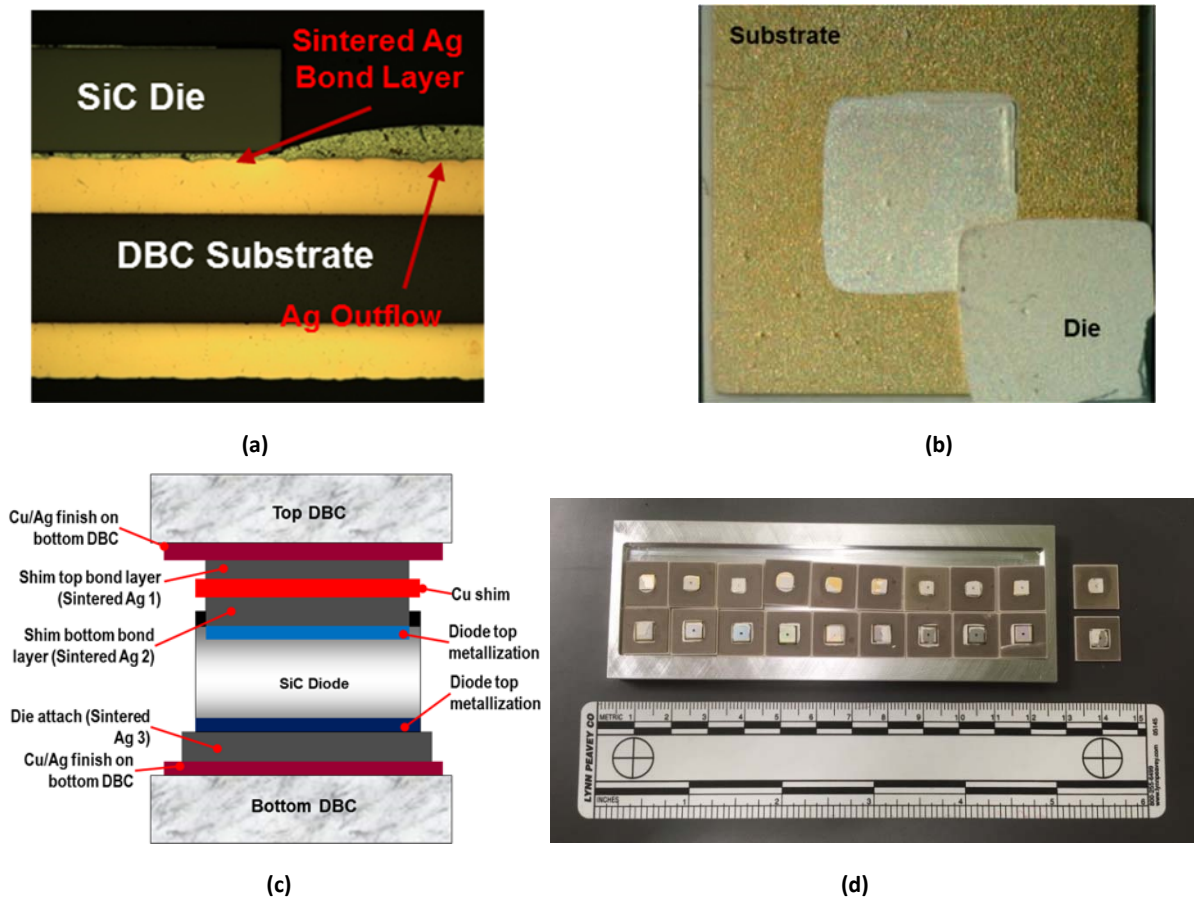


Figure 10: Experimental studies of silver sintered die bonds: (a) cross-sectional view of sintered silver bond of SiC die on DBS, (b) broken interface of bonded die on DBC, (c) three bond layers in planar package, and (d) photo of sheared off samples.

In experiments, the shear strength to break off the bond layers was measured and is summarized in Figure 11. It indicates that the die attach (sintered Ag 3) is the strongest bond with more than 50 MPa of shear strength. The shim top bonds (sintered Ag 1) are in the range of 15 to 25 MPa, while the shim bottom bonds (sintered Ag 2) are mainly in the 10 to 20 MPa range. The difference is attributed to the finishing metallization on each bonding surface. The finishing metallization is silver on the substrate; gold on all surfaces of the shim; and aluminum on the top of the SiC diode die, with silver on the bottom of it. Thus the sintered Ag 3 layer bonds both surfaces with silver finishing. The sintered Ag 2 bonds surfaces with silver and gold, while the sintered Ag 1 bonds surfaces with silver and gold. From these experiments, a conclusion can be drawn that silver metallization produces the strongest sintered silver bond, gold metallization produces acceptable bonds, and aluminum produces poor bonds.

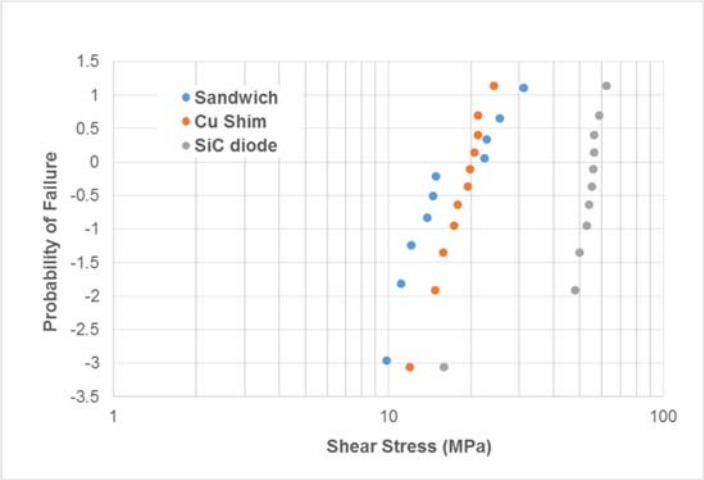


Figure 11: Shear strength of three bond layers.

Conclusions and Future Directions

Focusing on achieving a 40% cost reduction and 60% power density increase to facilitate DOE EDT 2022 power electronics targets ($3.3/kW, 14.1 kW/kg, 13.4 kW/L), the R&D on advanced packaging design and technology demonstrates the following.

1. Specially designed packaging technologies for fabrication of multiple device GaN power modules will allow an increase of 30% in the power density of a charger converter.
2. Limitations of state-of-the-art industrial packages would prevent achievement of the superior performance of WBG devices.
3. Ultralow inductance designs and prototypes demonstrated a record-low switching ringing SiC module that will greatly enhance the advantages of using WBG in inverters and converters.
4. Optimized area bonding technologies significantly improved the high-temperature reliability of SiC packaging for WBG power modules.

The achievements fulfill greatly the project objectives and the developed WBG packaging technologies result in leapfrogging barriers of existing industrial baseline and bring innovative, systemic development to electric drive systems

Future works include integration of these advanced packaging designs and technologies into building up of WBG systems and work together with industry to transfer them to manufacturers.

FY 2016 Presentations/Publications/Patents

Presentations/Publications

1. Zhiqiang Wang, Xiaojie Shi, Leon M. Tolbert, Fred Wang, Zhenxian Liang, Daniel Costinett, and Benjamin J. Blalock, "Temperature-dependent short-circuit capability of silicon carbide power MOSFETs," *IEEE Transactions on Power Electronics*, **31**(2), pp.1555–1566 February 2016.
2. Fei Yang, Zhenxian Liang, Zhiqiang Wang, and Fred Wang, "Parasitic inductance extraction and verification for 3D planar bond all module," presented at the International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM), June 13–15, 2016, Raleigh, North Carolina.
3. Zhenxian Liang, "Integrated double sided cooling packaging of planar SiC power modules," presented at the Seventh Annual IEEE Energy Conversion Congress and Exposition (ECCE 2015), September 20–24, 2015, Montreal, Canada.

4. Zhenxian Liang, "Survey of high density power electronics packaging technologies," presented at the United States Council for Automotive Research LLC, U.S. DRIVE Electrical and Electronics Technical Team meeting, July 21, 2016.
5. Zhenxian Liang, "Advanced packaging technologies and designs," presented at the DOE Vehicle Technologies Office 2016 Annual Merit Review, June 7, 2016, Washington, DC.
6. Zhenxian Liang, "Advanced packaging technologies and designs," presented at the United States Council for Automotive Research LLC, U.S. DRIVE Electrical and Electronics Technical Team meeting, April 26, 2016.
7. Zhenxian Liang, "Power packaging reliability test plan," presented at the United States Council for Automotive Research LLC, U.S. DRIVE Electrical and Electronics Technical Team meeting, February 25, 2016.
8. Zhenxian Liang, "Integrated packaging of SiC power modules," presented at the 3rd IEEE Workshop on Wide Bandgap Devices and Applications (WiPDA), November 2–5, 2015, Blacksburg, Virginia (panelist presentation).

Patents and Invention Disclosures

1. Zhenxian Liang, "Integrated packaging of multiple double sided cooling planar bond power modules," US Patent Application 62/167,371, filed for ID-3211, May 20, 2016.
2. Zhenxian Liang, Fei Yang, and Fei Wang, "Ultra-low parasitic inductance planar power module packaging," Invention disclosure 201603720, DOE S-138,365, August 15, 2016.

6.1 Power Electronics and Electric Motor Materials Support (Joint with VTO Propulsion Materials)

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Contract No.: DE-AC05-00OR22725

Abstract/Executive Summary

Materials research and development (R&D) support is provided to both power electronics (PE) and electric motor (EM) research efforts under way at NTRC via joint funding from the VTO Propulsion Materials and EDT Programs.

- PE materials support: The FY 2016 effort involved applied R&D of sinterable silver (Ag) as a candidate interconnect for PE devices and attempts to hasten the more confident adoption of sintered-Ag technology and consequent improvement in the reliability of automotive PE devices. Other EDT-sponsored PE packaging efforts at NTRC were supported and an ORNL-led collaborative effort with the National Renewable Energy Laboratory (NREL) occurred as well.
- EM materials support: Two primary R&D efforts occurred in FY 2016. The first effort involved investigation of new candidate potting compounds that could have better thermal transfer characteristics and higher- temperature capability and that are economically competitive. The second effort involved a fundamental study and measurement of the directional thermal transfer in copper (Cu) windings used in EMs, and involved an ORNL-led collaboration with NREL.

Accomplishments

- PE materials support (FY 2016 focus—sintered-silver interconnects)
  - Quantified achievable maximum strength.
  - Showed asymmetric residual stress can limit mechanical reliability.
  - Developed a proof test to identify the largest achievable interconnect size.
  - Showed shear strength was insensitive to the choice of plating, processing, and printing methods.
  - Showed sintered-Ag interconnects can be fatigue resistant.
  - Identified failure locations (weakest areas) in different sintered-Ag interconnect systems.
  - Weibull analysis and postmortem used to identify failure exclusivity and parasitics.

- EM materials support (FY 2016 focus—materials to promote thermal transfer in Cu windings)
  - Showed significant apparent thermal conductivity anisotropy of packed Cu wire.
  - Contrasted thermal conductivity test methods using Cu winding samples.
  - Used percolation theory to interpret thermal conductivity trends at higher wire-packing fractions.

✧ ✧ ✧ ✧ ✧

Introduction

For future PE devices, the potential use of sintered-Ag interconnection technology has several advantages over conventionally used solder-based interconnection technology (e.g., better electrical and thermal conductivity, microstructural equilibrium, potential for much better reliability). However, its adoption has been slow because it is a relatively new technology and the PE community is relatively conservative. This VTO Propulsion Materials–EDT jointly funded effort seeks to hasten the more confident adoption of sintered-Ag by identifying the achievable strength characteristics of such interconnect systems, which are relatively complex (Figure 1). This effort will guide future sintered-Ag design for PE and improve the PE community's receptiveness to adopting sintered-Ag technology.

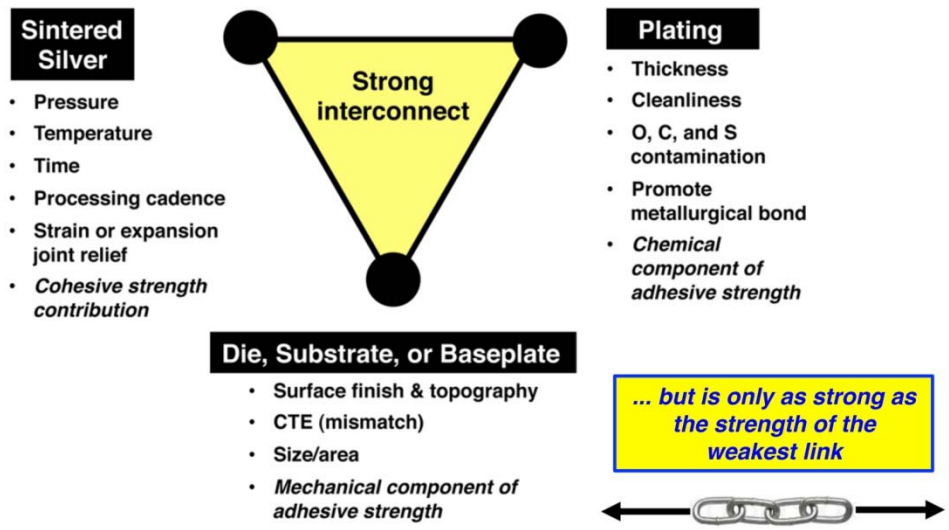


Figure 1: The strength and reliability of a sintered-Ag interconnect is a function of many parameters.

Minimizing the service temperature in Cu windings in EM slot liners will promote greater efficiency and enable EM size and weight reductions. Such wires in slot liners are shown in Figure 2. Two ways to achieve minimization are by using more thermally conductive materials in EMs and by improving the understanding of the anisotropic thermal transfer within those Cu windings. New potting and molding compounds that have better thermal transfer characteristics and higher temperature capability are attractive candidates for this purpose, provided they are cost competitive and do not introduce performance compromises. Greater understanding of the thermal transfer characteristics starts with the fundamental study and measurement of the directional thermal transfer in Cu windings used in EMs; however, specimens that represent how these Cu windings thermally respond in service must be developed and thermally measured.

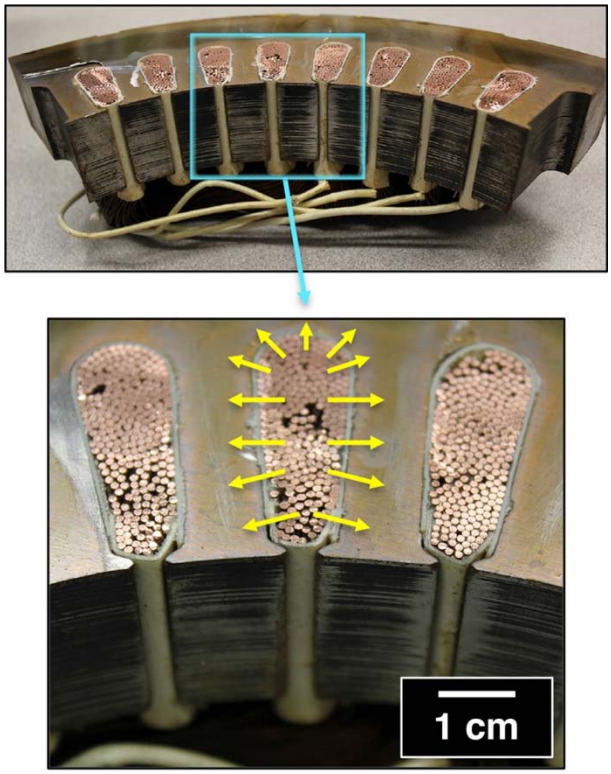


Figure 2: Sectioned view showing Cu-wire packing within slot liners. Yellow arrows represent the direction of potential heat transfer from the Cu wires.

Approach

PE Materials Support

- Fabricate sintered-Ag test coupons that enable the measurement of a critical dependent parameter associated with interconnect reliability and shear strength, and measure it as a function of the plating material [Ag vs. gold (Au)], drying method, and printing method (screen vs. stencil).
  - Perform postmortem failure analysis to identify failure location and failure type.
  - Publish results and interpretations.
- Coordinate and lead a sintered-Ag thermomechanical reliability study with NREL.
  - Examine the effect of coefficient-of-thermal-expansion (CTE) –induced residual stress on sintered-Ag printed pad size and the onset of delamination of the interconnect.
  - Fabricate all specimens and provide materials characterization analysis.
  - Publish results and interpretations.

EM Materials Support

- Fabricate Cu-wire-wound test coupons with filler materials that will promote greater thermal conductivity perpendicular to the wires.
  - Publish results and interpretations.
- Coordinate and lead a collaboration with NREL to better understand the directional thermal response of Cu-wound structures.
  - Fabricate test specimens that facilitate the valid measurement of thermal diffusivity and thermal conductivity as a function of wire orientation.
  - Use different methods of thermal property measurement to enable comparisons, and validate the legitimacy of the results.
  - Publish results and interpretations.

Results and Discussion

PE Materials Support

Maximum Size

A simple and inexpensive approach was developed to identify the largest achievable interconnect size with sinterable Ag. That size is an outcome of all the cumulative effects of numerous independent parameters that each affects that achievable size. The method can be viewed as a proof test. The method involves making geometrically simple test coupons whose materials have CTEs that match or mimic those of materials used in PE devices and that are bonded by an interconnect material whose bond size is likely to exceed that used in that device. Figure 3 is a schematic of the geometries and materials used in this study.

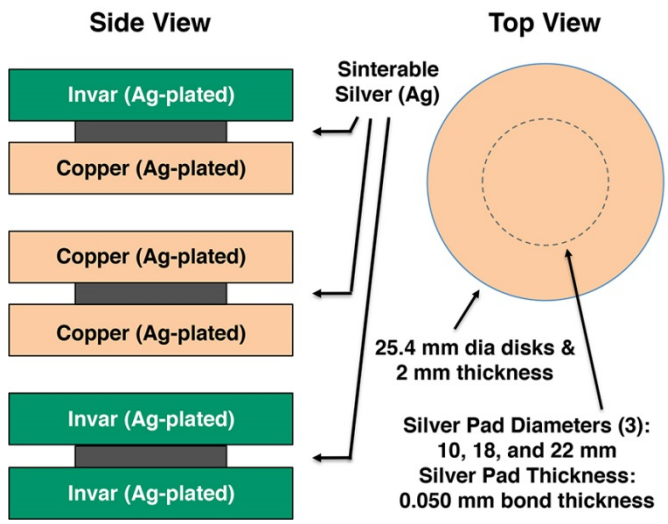


Figure 3: Schematic showing how CTE-induced residual stress was purposely varied through choice of disk materials and bonding size.

Delamination occurred simply from the cooldown to room temperature from the 250°C bonding process for the Cu-invar couple when they were bonded with 18 and 22 mm diameter sintered-Ag pads. Delamination did not occur in this stage for this couple when 10 mm diameter sintered-Ag pads bonded the Cu and invar.

A large differential in the CTE mismatch relative to the sintered-Ag would cause delamination for larger bonded areas (i.e., the Ag-bonded invar-invar couples); however, an asymmetric CTE across (or perpendicular to the interconnect plane of) the sintered-Ag interconnect is more apt to promote the onset of delamination. Such across-the-interconnect CTE asymmetry superimposes in-plane and out-of-plane shear stress resulting in an overall higher (equivalent) stress that is more likely to reach the interconnect system's shear strength and cause the onset of delamination. Examples of delaminations as a function of size for the Cu-invar couple are shown in Figures 4 and 5.

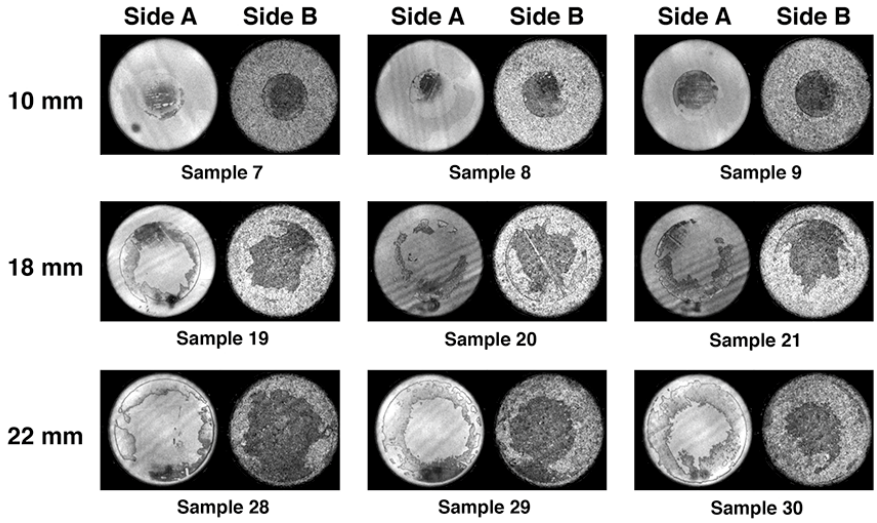


Figure 4: Acoustic microscopy images of the as-processed Cu-invar couples bonded with Ag. Each of the nine pairings consists of images captured through opposite directions. Disks are 25 mm in diameter.

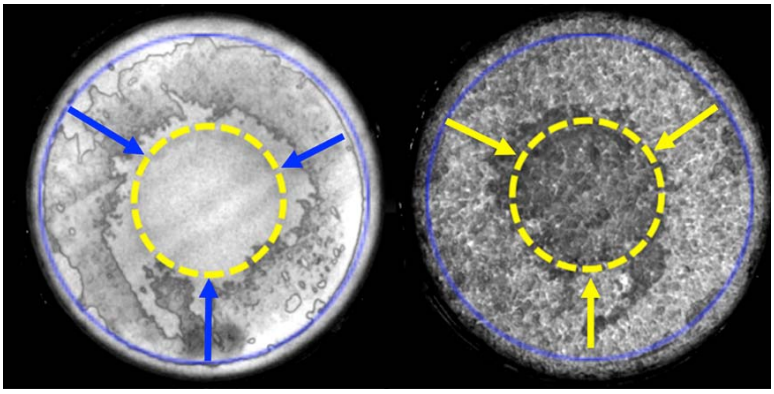


Figure 5: Example of superimposed (dashed) circles on a Cu-invar couple used in the analysis of the sustained sintered-Ag bond shape. The arrows show the radial ingress from the original printed diameter. Disks are 25 mm in diameter.

Thermal cycling (entire coupon at an isothermal temperature for any given temperature of that cycling) caused mortality of all the Cu-invar couples by 400 cycles (Figure 6). This suggests that subjecting such an interconnect system to a relatively low number of thermal cycles could serve as an effective proof test. Such thermal cycling did not cause failure for Cu-Cu or invar-invar couples bonded by sintered-Ag (up to 22 mm diameter print pads); this further illustrates the deleterious influence of an asymmetric CTE mismatch across the sintered-Ag interconnect.

Interpretation of the tracking of the delamination of the thermal-cycling-induced failures suggests that the sintered-Ag process used here produced a relatively fatigue-resistant interconnect. That statement is based on the absence of identifiable continuous delamination up to failure of the interconnect system (i.e., catastrophic delamination must have initiated and entirely occurred in less than 100 cycles); this is an indicator of a relatively high fatigue exponent.

A sintered-Ag interconnect having a diameter of at least 22 mm can bond Cu to Cu, and a sintered-Ag interconnect of at least 10 mm can bond invar to invar. A 10 mm diameter sintered-Ag interconnect will fail in thermal cycling if it bonds Cu to invar. Sintered-Ag bondability with other material pairings [e.g., silicon, aluminum, molybdenum, and direct bond copper (DBC) substrates] based on the respective CTEs of the materials has also been considered.

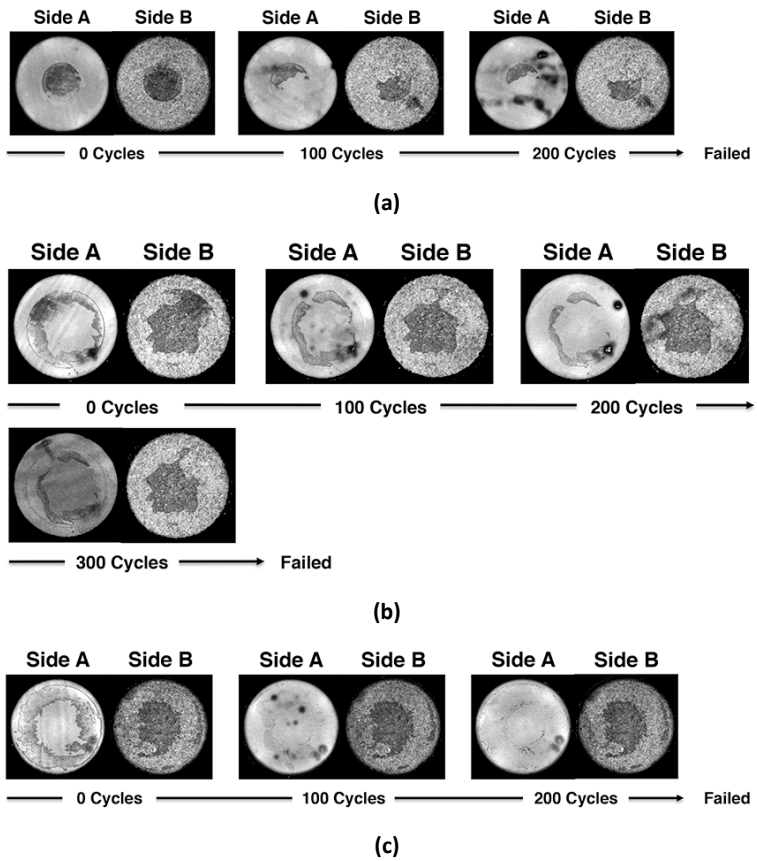


Figure 6: Tracked acoustic microscopy images of (a) 10 mm diameter, (b) 18 mm diameter, and (c) 22 mm diameter bonded Cu-invar couples. All failed in less than 400 thermal cycles.

Plating, Processing, and Failure Interpretation

Shear strength of the explored sintered-Ag interconnect system was insensitive to the choice of Au or Ag as plating material, processing method (predrying vs. wet-surface-consolidation), and printing method. Sintered-Ag interconnect systems should be able to withstand shear stresses of ~30 MPa if consistent processing (i.e., no exclusive flaw types) is used (Figure 7). They will fail if service shear stresses exceed ~ 60 MPa.

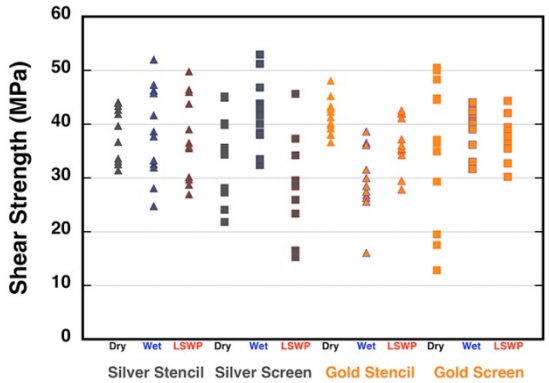


Figure 7: With the exception of some low-strength outliers, the majority of shear strengths were greater than 25–30 MPa.

Despite shear strength being insensitive to the processing method, compromised print-pad structure can be introduced with predried, screen-printed, and wet-processed sintered-Ag, and that can manifest itself in relatively low shear strength of the interconnects. Because sintered-Ag is still undergoing process development, the use of combined Weibull and failure analyses can be useful in identifying exclusivity and

parasitics associated with its process development and testing. The change-in-slope at lower strength values in the Weibull plot (Figure 8) is an illustration of such compromise.

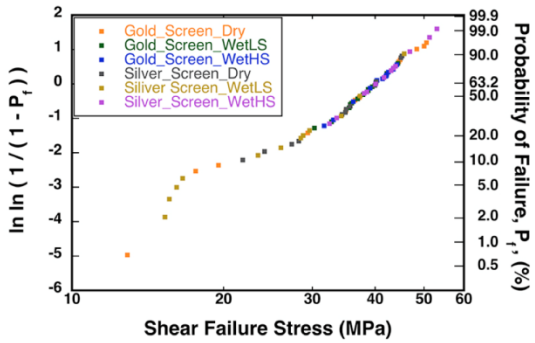


Figure 8: Change in slope at failure stresses < 20 MPa is an indication of operative exclusive flaw types.

Ag-plated DBC sandwiches tended to adhesively fail between the Ag plating and DBC cladding. Gold-plated DBC sandwiches tended to fail in a hybrid manner, with the majority of failure resulting from cohesive failure of the sintered-Ag bond with additional adhesive failure between the Au plating and the nickel-phosphorus (Ni-P) sublayer.

EM Materials Support

EM materials support included investigating materials to promote thermal transfer in Cu windings. The anisotropic apparent thermal conductivity of packed Cu wire can be satisfactorily estimated with appropriate specimen preparation and use of the laser flash and transmittance test methods. The transient hot disk method did not consistently produce trustworthy and defendable apparent thermal conductivity results for the Cu wire specimens and their architecture. Test specimens and methods are shown in Figure 9.

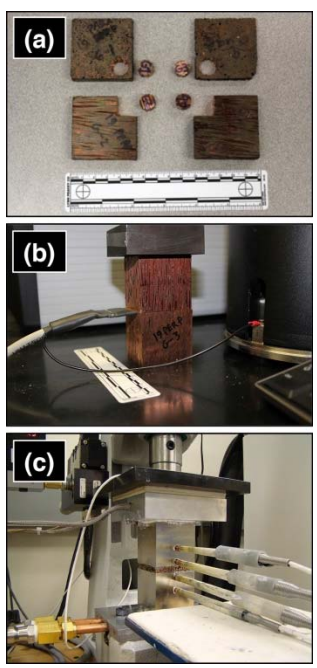


Figure 9: Test specimen harvesting for (a) laser flash testing and test setups for (b) transient plane source and (c) thermal transmission testing.

The apparent thermal conductivity of the packed Cu wire was about 2 orders of magnitude higher in the direction parallel to the wires than perpendicular to them. The former was more than 200 W/mK while the latter was only 0.5 to 1 W/mK for a wire packing efficiency of about 50%. Results are shown in Table 1.

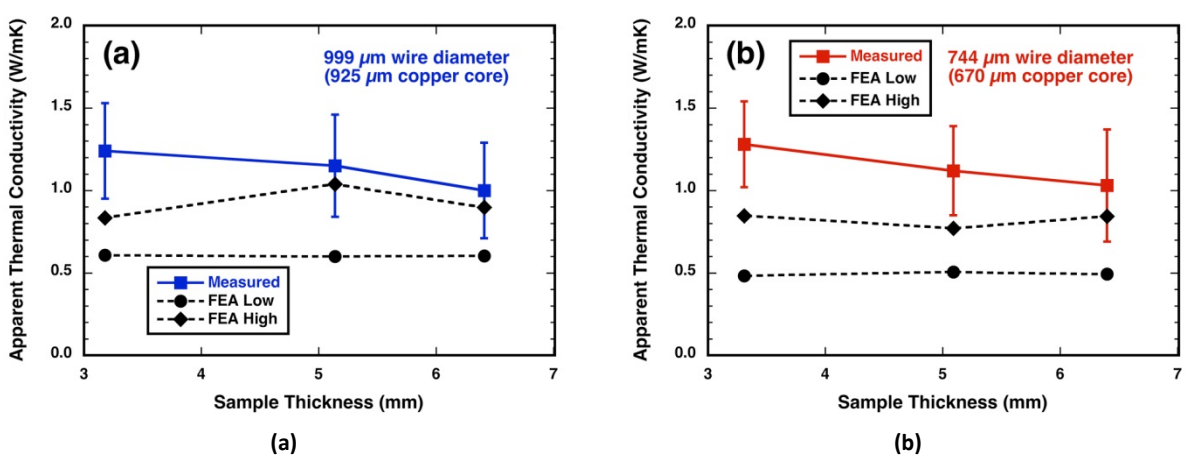
Table 1: Measured thermal conductivities as a function of test method

Material	Apparent Thermal Conductivity κ_app (W/mK)		
	Laser Flash E1461	Transient Plane Source ISO 22007-2	Thermal Transmittance ASTM D5470
Cu-Wire & Varnish, Parallel or Longitudinal, 19-Ga	238	[a]	
Cu-Wire & Varnish, Perpendicular or Transverse, 19-Ga	0.55	[a]	1.0–1.2
Cu-Wire & Varnish, Parallel or Longitudinal, 22-Ga	212	[a]	
Cu-Wire & Varnish, Perpendicular or Transverse, 22-Ga	0.52	[a]	1.0–1.2
Varnish[b]		0.19	

[a]Technique unfavorable for highly anisotropic materials.
[b]Actual κ measured (not κ_app).

The measured apparent thermal conductivity responses of the packed Cu wires consisting of either 670 or 925 µm diameter wires did not exhibit significant differences in the direction perpendicular to the wires at a packing efficiency of ~ 50%. The Kanzaki model's prediction of apparent thermal conductivity differences for their combinations also indicates an equivalence [1]. However, the apparent thermal conductivity parallel to the wires for the 925 µm diameter wires was nearly 10% higher than that for the wire packs containing the 670 µm diameter wires.

For the transmittance test method, the average apparent thermal conductivity perpendicular to the wires and the amount of scatter were insensitive to specimen thickness for thicknesses from 3.2 to 6.4 mm. This is illustrated in Figure 10. It is believed this thickness range constitutes a size smaller than the representative volume element for these packed Cu wire systems; therefore, the amount of scatter in the measured apparent thermal conductivity could be greater or less as the thickness gets smaller or larger.



(a) (b)

Figure 10: Apparent thermal conductivity perpendicular to wires as a function of sample thickness using transmittance test method for (a) 925 µm diameter or 19 Ga and (b) 670 µm diameter or 22 Ga Cu core wires. Indicated bars on the measurements represent 95% confidence bands. Finite element analysis (FEA) low and high bounds represent fill factors from density and image analysis estimations, respectively.

Percolation channels (Figure 11), representing localized pathways having relatively high concentrations of Cu, likely caused the packed Cu wire to have a slightly higher apparent thermal conductivity than that predicted by finite element analysis (FEA).

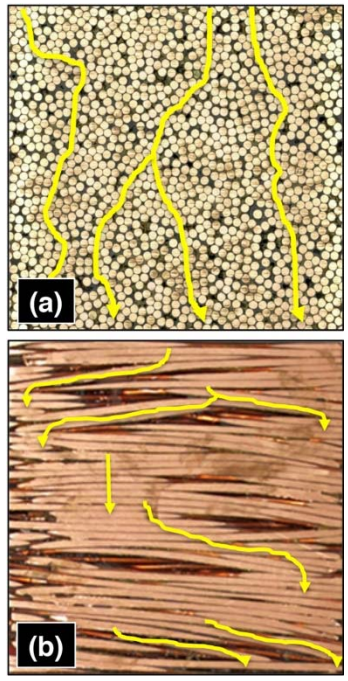


Figure 11: Percolation pathways (yellow) that potentially provide localized preferential thermal conduction. Potential pathways are illustrated for two mutually orthogonal sections of packed Cu wire [(a) and (b)].

The Kanzaki model (with FEA confirmation) provides a satisfactory numerical estimation of the apparent thermal conductivity of the packed Cu wire in the direction perpendicular to the oriented wires. This estimation takes into account the wire diameter and its thermal conductivity, the wire insulation coating thickness and its thermal conductivity, and the packing factor and the thermal conductivity of the interstices material. The model supports the expectations that increasing the thermal conductivity of both the wire insulating coating material and the material in the interstices can significantly increase the apparent thermal conductivity perpendicular to the wire orientation in packs of aligned Cu wire. This is illustrated in Figure 12.

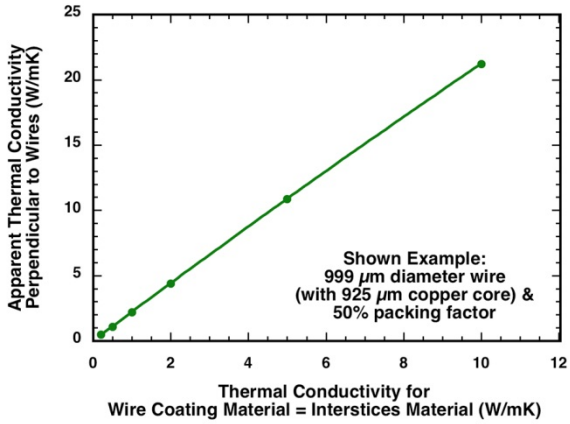


Figure 12: Calculated apparent thermal conductivity perpendicular to the wires as a function of thermal conductivity of the wire coating material and interstices material (after [1]). The thermal conductivities of the wire coating material and interstices material are set equal in this example.

Conclusions and Future Directions

Conclusions

- PE materials
  - Maximum strength. Sintered-Ag interconnect systems should be able to withstand shear stresses of ~30 MPa if consistent processing is used. They will fail if service stresses exceed ~ 60 MPa.
  - Asymmetric residual stress. Asymmetric CTE across (or perpendicular to) an interconnect's plane is more apt to promote the onset of delamination. Such an oriented stress state superimposes in-plane and out-of-plane shear stress resulting in higher (equivalent) stress that is more likely to reach the interconnect system's shear strength and cause the onset of delamination.
  - Proof testing. A simple and inexpensive approach was developed to identify the largest achievable interconnect size with sintered-Ag. The method can be considered as a proof test.
  - Shear-strength insensitivity. Shear strength of the explored sintered-Ag interconnect system was insensitive to the choice of Au or Ag as plating material, processing method (predrying vs. wet-surface-consolidation), and printing method (screen vs. stencil).
  - Fatigue resistance. Sintered-Ag was determined to be a relatively fatigue-resistant interconnect. There was no identifiable continuous delamination occurring up to failure of the interconnect system; this is an indicator of a relatively high fatigue exponent.
  - Failure location. Silver-plated DBC sandwiches tended to adhesively fail between the Ag plating and DBC cladding whereas Au-plated DBC sandwiches tended to fail in a hybrid manner, with the majority of failures resulting from cohesive failure of the sintered-Ag bond with additional adhesive failure between the Au plating and the Ni-P sublayer.
  - Failure analysis. The use of combined Weibull and postmortem failure analyses can be useful in identifying exclusivity and parasitics associated with sintered-Ag process development and testing or both.

- EM materials
  - Anisotropy. Identified that the apparent thermal conductivity of packed Cu wire was about 2 orders of magnitude higher in the direction parallel to the wires than perpendicular to them. The former was more than 200 W/mK while the latter was only 0.5 to 1 W/mK for a wire packing efficiency of about 50%.
  - Test methods. The anisotropic apparent thermal conductivity of packed Cu wire can be satisfactorily estimated with appropriate specimen preparation and use with the laser flash and transmittance test methods. The transient hot disk method did not consistently produce trustworthy and defendable apparent thermal conductivity results for these specimens and their architecture.
  - Specimen size. The average apparent thermal conductivity perpendicular to the wires and the amount of scatter were insensitive to specimen thickness (for thicknesses 3.2 to 6.4 mm) for the transmittance test method. It is believed this thickness range constitutes a size smaller than the representative volume element for these packed Cu wire systems; therefore, the amount of scatter in the measured apparent thermal conductivity could be greater or less as the thickness gets smaller or larger.
  - Percolation. Percolation channels, representing localized pathways having relatively high concentrations of Cu, likely cause packed Cu wire to have a slightly higher apparent thermal conductivity than that predicted by FEA.

Future Directions

- Paste drying. Refine new ORNL-developed method to dry sinterable-Ag paste. It enables strong interconnect bonding without the need for concurrent pressure and the use of reflow oven processing.
- Sintering with reflow oven. Refine sintered-Ag interconnect processing method using reflow oven processing technology.

- Shear and tension. Complete study and mechanical test method development to examine how shear or tension stress states or both affect strength of sintered-Ag interconnects.
- Fracture toughness. Complete study and mechanical test method to estimate the apparent fracture toughness of sintered-Ag interconnects.
- Silver plating. Examine mechanical integrity of Ag plating used with sintered-Ag interconnects.
- Thermally conductive fill. Complete study on candidate thermally conductive fill materials.

FY 2016 Presentations/Publications/Patents

1. A. A. Wereszczak, J. E. Cousineau, K. Bennion, H. Wang, R. H. Wiles, T. B. Burress, and T. Wu, "Anisotropic thermal response of packed copper wire," in review, *Journal of Thermal Science and Engineering Applications*, 2016.
2. A. A. Wereszczak, M. C. Modugno, S. B. Waters, D. J. DeVoto, and P. P. Paret, "Method to determine maximum allowable sinterable silver interconnect size," in *IMAPS HiTEC 2016*, Paper WP23, May 10–12, 2016, Albuquerque, New Mexico, pp. 207–215.
3. M. C. Modugno, A. A. Wereszczak, and S. B. Waters, "Toward interpreting failure in sintered-silver interconnection systems," in *IMAPS HiTEC 2016*, Paper WP26, May 10–12, 2016, Albuquerque, New Mexico, pp. 234–241.
4. T. Wu, A. A. Wereszczak, H. Wang, B. Ozpineci, and C. Ayers, "Thermal response of an additive manufactured aluminum," presented at the *International Symposium on 3D Power Electronics Integration and Manufacturing*, June 13–15, 2016, Raleigh, North Carolina.
5. "Method to Determine Maximum Allowable Sinterable Silver Interconnect Size," presented at *IMAPS HiTEC 2016*, May 10–12, 2016, Albuquerque, New Mexico,.
6. "Sintered silver R&D at ORNL," presented at the United States Council for Automotive Research LLC, U.S. DRIVE Electrical and Electronics Technical Team meeting, March 17, 2016, Southfield, Michigan.
7. "Materials introspections," presented at the EDT Research Industry Engagement Meeting, October 28, 2015, Knoxville, Tennessee.

References

1. H. Kanzaki, K. Sato, and M. Kumagai, "A Study of a Technique to Predict the Equivalent Thermal Conductivity of an Electric Coil," *Transactions of the Japan Society of Mechanical Engineers, Series B*, **56**(526) pp. 1753–58, 1990.